analog dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

Volume 21, Number 2, 1987

ANALOG DEVICES

Editor's Notes

IT'S YOUR TURN

"The space below has been intentionally left blank" is a statement you'll find occasionally in a variety of documents, but hardly ever in a serious publication of news or ideas, since the implication would be that the editor or publisher has run out of thoughts—and that's unthinkable!

In this case, we'd like to keep bringing tangible meaning to the name of our publication. We want to give you an optimum chance to talk back, to let us know who's out there and what you think is OK and not-so-OK about us, what you think we should keep on doing, what we should stop doing, what we should *start* doing.

So here's some blank space to get started on. You can write here and tear the page out—better yet, if you share our antipathy towards vandalism of worthy publications, make a copy of this page and write, using both sides of the copy paper if necessary (you have our express permission to copy for this purpose). Even better, treat the space as symbolic and use your letterhead. Send it to the address below, attention of the undersigned.

The blank space is for *you*. So start writing.

Dan Sheingold

THE AUTHORS

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analog dialogue

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ISSN 0161–3626

COMPLETE MONOLITHIC 8-BIT 400-ksps ANALOG I/O SYSTEM

AD7569 Combines ADC, DAC, Bus Interface & Associated Functions In Single Plastic or Ceramic "Skinny DIP" or Leaded Chip Carrier

by Mike Byrne and Mike Tuthill

Input/output (I/O) ports have long been available in monolithic form for serial communications and other digital functions. Now the AD7569 provides designers with a complete, easy-to-use 8-bit *analog* I/O port in a single small package containing a high-performance, fully specified (for both time and frequency domains) CMOS chip. Applications for it exist wherever analog signals must be converted and flow freely to and from a digital system. It is especially useful in control, where data must be independently acquired from a real-world transducer, analyzed and processed, and the results used to generate a controlling or correcting analog signal for output to the real world.

Typical applications include servo loops, autocalibration systems, disk-drive head-position controllers, and HVAC (heating, ventilating, and air conditioning) controls. In addition, there are useful occasions where a complete control loop can be built without a processor, or an improved circuit function realized by teaming up an a/d and a d/a converter.

The AD7569, Figure 1, combines on a single monolithic chip everything needed to interface an 8-bit microprocessor bus to the analog world: a 400-ksps sampling ADC, a separate 2-µs DAC, and a digital bus interface—along with the necessary ranging, track/hold, clocking, and voltage-reference circuitry. No external components or user trims are required. Since the overall system accuracy is fully specified, there is no need to calculate error budgets from the indvidual sub-function error specifications.

Dynamic performance is designated in terms of both frequency specifications—oriented to digital signal-processing (DSP)—and the traditional time-domain specifications. Examples of the former include signal-to-noise ratio, distortion, and input bandwidth. The bus interface timing is very fast, eliminating the need for *wait* states during ADC *Read* or DAC *Write* for most microprocessors. A separate *Start Convert* line controls the track/hold to allow precise control of the sampling time and start of conversion. Because of the small package size—24 pin "skinny" (0.3") DIP or 28-terminal chip carrier—these benefits are inherent for high-density circuitry; in addition, the low power dissipation of

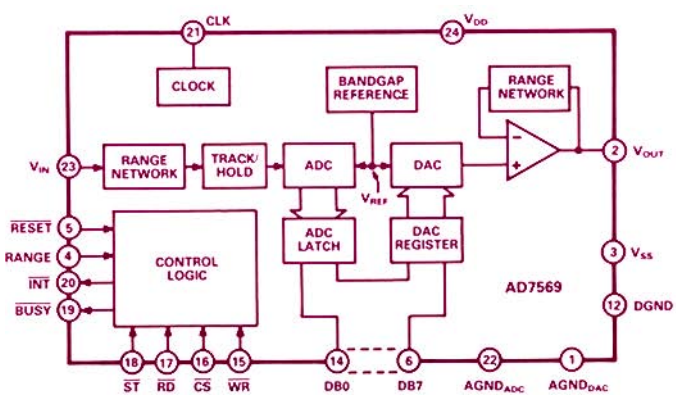
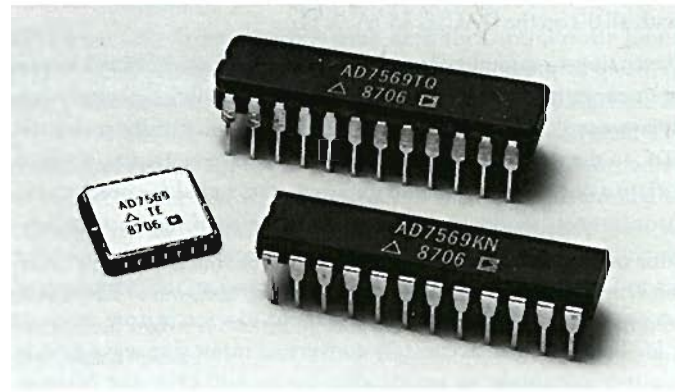


Figure 1. Functional block diagram of the AD7569.

*Use the reply card for technical data.



CMOS (<80mW maximum) and low supply-current requirements minimize heat problems in these designs. The price of this component is less than the cost of buying, assembling, and testing the individual functional elements—only $6 in 100s.

ARCHITECTURE

The internal design of the AD7569 comprises building blocks and the required collateral circuitry for the complete analog I/O system. Linear-compatible CMOS (LC^2MOS) fabrication combines the precision of bipolar analog circuits with the low power requirements of CMOS logic. A low-noise, trimmed, temperature-compensated bandgap reference is used for both the 8-bit output DAC and the identical (but independent) DAC used as the heart of the successive-approximation ADC. Control logic manages the IC functions and the bus interface.

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The DAC output is buffered by a high-speed op amp that can develop up to ±2.5 V across a 2-kΩ, 100-pF load. The feedback path of this buffer contains a gain/offset network for a choice of four output voltage ranges, set by the *Range* pin and the V_{SS} supply value. With a single +5-volt supply, output ranges are 0 to +1.25 V and 0 to +2.5 V; with a dual supply of ±5 V, the output ranges are ±1.25 V and ±2.5 V. At full scale, the output noise of the DAC is 200 μV peak-to-peak (p-p); the spot noise at 1kHz (with all 0's on the DAC) is 35 nV/$\sqrt{Hz}$.

The analog-to-digital-conversion subsystem of the AD7569 has an input-range network, track/hold, ADC, and an internal clock (not always used). The input range circuitry automatically scales the ADC to the same span as the DAC output. There are two ways to initiate a conversion: with an external *start* signal for precise synchronization (mode 1) or by a processor *read* memory cycle—which brings both the *Chip-Select* and *Read* control lines of the bus to the active state (mode 2). In either mode, the beginning of a conversion cycle causes the track/hold to switch from *track* to *hold*. The ADC can accurately convert an input sine wave of 2.5-volt p-p amplitude at frequencies up to 100 kHz, the Nyquist frequency of the ADC when operating at a throughput rate of 200,000 samples per second.

In mode 1, the conversion begins as soon as the *start* signal is received. During the conversion period the *Busy* line indicates that a conversion is in progress; at the end of conversion the *Busy* line goes back to the inactive state, an interrupt (INT) signal is generated (to indicate to the processor that a conversion has been completed), and the track/hold circuit reverts to the *track* mode. The INT line is reset when the result of the conversion is read out of the ADC latch—or when the entire chip is reset. In mode 2, the processor *read* cycle initiates the conversion, and the processor must be put into a *wait* state during the conversion cycle; this is done by connecting the *Busy* line to the processor's *Ready*—or *Wait*—input. At the end of the conversion cycle, the *read* operation is completed when the new conversion result is placed on the data bus.

The choice between mode 1 and mode 2 involves a tradeoff in application performance. In mode 1, the conversion can be initiated at precise intervals that are beyond the direct control of the processor; an interrupt service routine is used to retrieve the results of conversion. In mode 2, the processor can begin conversion simply by executing a *read* cycle, but the uncertain timing of the start of each *read* cycle doesn't permit uniform sampling; also, the processor is wasting time while the conversion takes place.

The interface between the AD7569 and the processor bus is straightforward, managed by the same control logic that controls the DAC and ADC operations. Either TTL or 5-volt CMOS levels can be used. The DAC register is loaded as eight parallel bits, under control of the *Chip Select* and *Write* lines. Data from the bus is transferred into the DAC register when the *Write* line goes from the active to the inactive state; this edge-triggering keeps the DAC register opaque at all other times. The *write* signal can be as short as 80 ns, compatible with most of the faster processors. When the IC's *Reset* line is set *low*, all-0s are loaded into the DAC register; this results in 0 volts out for unipolar output and negative full-scale for bipolar output. The ADC latch is accessed by simple memory *read* cycles, at the same address as the write cycles, with only a 60-ns *read* pulse needed.

The AD7569 requires a clock for the successive-approximation conversion process and other internal timing needs. It can be generated by an internal circuit, with an external resistor and capacitor connected in parallel between the CLK pin and ground. This convenient clock source is adequate for many purposes, but the actual operating frequency may vary by up to ±25% from device to device, decreasing as the chip temperature rises. For greater precision and stability, an external clock can be supplied; it may run continuously and need not be disabled between conversion cycles.

SPECIFICATIONS

Even though a great many functions are combined on the AD7569, the performance achieved for each function individually is impressive. For the highest- grade version (K suffix), the DAC has a relative accuracy of better than ±½ LSB, with maximum differential nonlinearity of ±¼ LSB. All grades are guaranteed monotonic. The total unadjusted error—a comprehensive specification that embraces the internal voltage-reference error, relative-accuracy error, and gain and offset errors—is ±2 bits. The ADC has similar relative accuracy and differential nonlinearity specifications, and its total unadjusted error is ±3 bits.

The AD7569's ac parameters are also specified: they include signal-to-noise log-ratio (SNR), harmonic and intermodulation distortion, and input bandwidth. These specifications are especially critical for digital signal-processing (DSP) applications (see the article starting on p.6 of this issue for a discussion of these specifications and their importance). The SNR and total harmonic distortion (THD) are specified with the DAC generating a 20-kHz sine wave sampled at 400 kHz. This is done by loading the DAC with the 8-bit codes corresponding to an ideal sine wave at precisely timed angular intervals. The first six harmonics in the output of a DAC, updating at 400 kHz and generating an 8-kHz sine wave, are shown in the spectral density plot of Figure 2.

The DAC's SNR can be computed from the log product of the (white) noise spectral density (about 93 dB below the normalized 1st harmonic) and the square root of the normalized 50-kHz bandwidth; the result is −46dB. The THD is better than −48dB, measured by the ratio of the rms sum of the 2nd through 5th harmonics to the fundamental (1st harmonic) value. For intermodulation distortion (IMD) tests, the numeric representation of summed sine waves at 18.4 kHz and 14.5 kHz—sampled at 400 kHz—is used. IMD for the AD7569's DAC is typically −55dB.

To test the dynamic performance of the *a/d converter*, a low-distortion sine wave is fed into the analog input of the AD7569

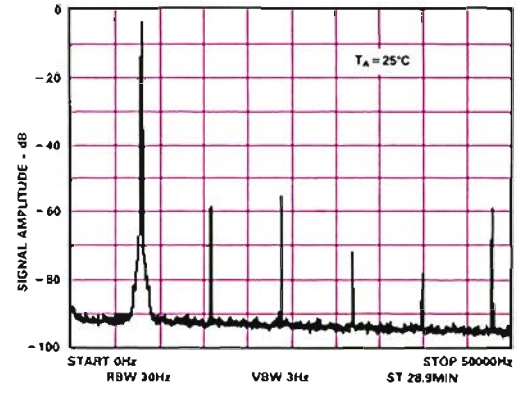


Figure 2. The DAC Output Spectrum for 8-kHz output, using a swept filter analyzer with 3-Hz filter bandwidth.

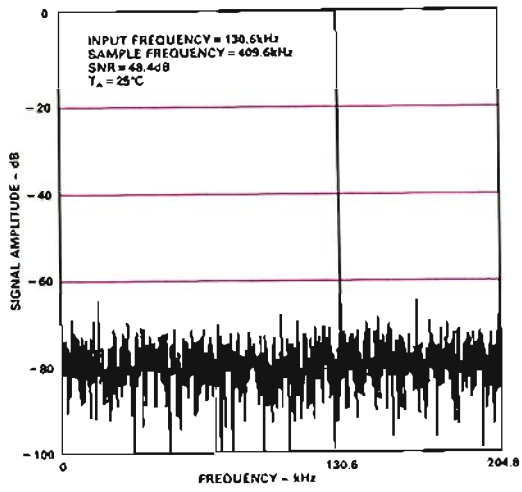


Figure 3. FFT plot of ADC performance, with input of 130.6 kHz, and sampling at 409.6 kHz.

and sampled at a rate greater than the Nyquist rate (i.e., *oversampled*). Then fast Fourier-transform (FFT) and histogram plots are generated to allow SNR, THD, and dynamic differential nonlinearity to be determined. Figure 3 shows the 2,048-point FFT plot for an input signal at 130.6 kHz, with sampling at 409.6 kHz. The SNR is 48.8dB (the rms fundamental magnitude to rms sum of all nonfundamental signals up to one-half the sampling frequency) which is within 1.2 dB of the theoretical ideal of 50 dB. From the SNR, the effective resolution can be derived; for this test, it is between 7.7 and 7.8 bits (out of a possible 8).

IMD can be analyzed in similar fashion from an FFT that shows the magnitudes of error signals at sum- and difference frequencies of a pair of pure sine waves applied to the voltage input of the ADC.

APPLICATIONS

The AD7569 can be used for any 8-bit bus application calling for independent a/d and d/a conversion. Many of its applications are in data acquisition and control; the ADC acquires and digitizes the data, a processor makes decisions based on the acquired data, and controlling outputs are generated via the DAC. The microprocessor's address, data, and control bus signals interface with the AD7569's corresponding signals (Figure 4). Conversion is initiated by the *start conversion* signal (mode 1) or a processor read cycle at the hard-wired address of the IC (mode 2). The end of conversion is signalled to the processor by the *interrupt* in mode 1; it initiates a service routine that reads the data. In mode 2, the converter's *Busy* signal puts the processor into a wait state, which ends when the conversion is complete, at which point the processor completes the extended *read* cycle (which initiated conversion) by acquiring the newly converted data.

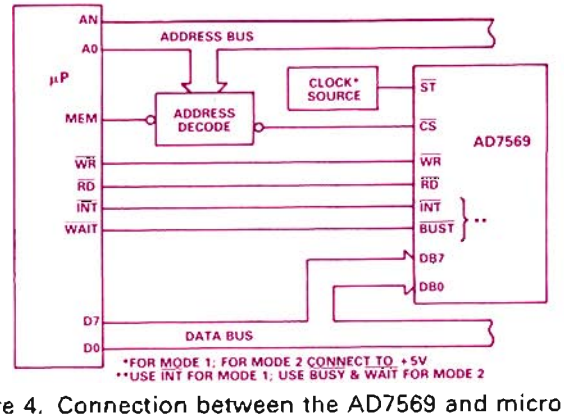


Figure 4. Connection between the AD7569 and microprocessor busses, for both periodic clock and read-cycle-initiated conversions.

Besides such conventional applications, the high level of functionality of this single chip—and its ease of interfacing—makes it ideal for some applications where *no processor* is involved. Here are a couple of examples:

•*Peak (or valley) detection.* A peak detector continuously monitors a signal (often representing temperature, pressure, speed, or flow), and retains the highest value that the signal reaches. As greater values are reached, they replace the previous value. The traditional analog approach uses a peak-holding capacitor, an op amp, and a comparator; the accuracy of the reading is limited by "droop" of the capacitor voltage. The digital method uses an ADC, processor, and software to continuously convert and compare signal values, but the processor and ADC are inefficiently utilized—and high oversampling rates are required so as not to miss the "actual" peak.

The circuit of Figure 5, which avoids using a processor for peak-detection, employs the AD7569 to detect and hold peak values indefinitely without droop; the peak value, which can be read either digitally or by an analog meter, is stored in the a/d converter and the DAC. The DAC's output sets the comparator's threshold level. When the input signal exceeds the stored value, the output of the TL311 comparator goes low, triggering the 74121 one-shot. This starts a conversion cycle; the result of the conversion is stored in the DAC and sets the new comparator-threshold level. The peak- detection function can be reset for a new detection period by using the *Reset* line of the AD7569. The *reset* can be controlled by software or a mechanical reset switch.

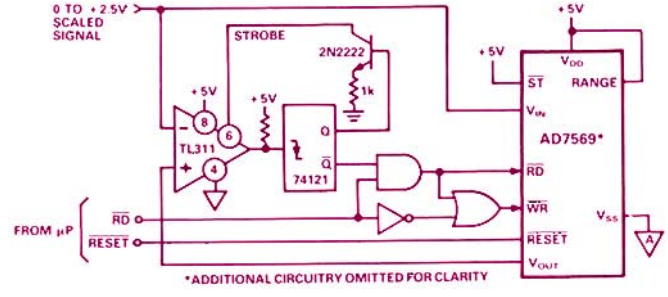


Figure 5. Peak-reading circuit uses the functions of the AD7569, requires no processor or software support, and has no droop.

•*High-precision oscillators* require constant output frequency; the crystal can be kept in a constant-temperature oven to achieve this, a power-hungry and relatively bulky approach requiring temperature-control circuitry. Alternatively, compact oscillators can be built using the AD7569, which—save for the PROM and temperature sensor—contains nearly everything required to *compensate* for temperature variations. Factory-determined correction factors are stored in a PROM look-up table. In field operation, the ADC output (representing measured temperature) is the PROM address, which points to a table entry. The correction factor stored at this address is applied to the DAC, whose output controls the voltage on a variable-capacitance tuning diode in parallel with the crystal. The resonant frequency of the crystal is "pulled" by the diode to correct for any temperature variations observed in calibration.

MONOLITHIC 10-BIT, 20-μs SAMPLING A/D CONVERTER

AD7579/AD7580 Combine Speed and 8/16-Bit Bus Interface

Fully Specified for Dynamic AC Performance

by Trevor Emmens

The AD7579 and AD7580* are 10-bit analog-to-digital converters designed to provide data acquisition of signals with fully specified dynamic performance and a minimum of additional components. The on-chip sample-hold function simplifies the data-acquisition system wiring and allows conversion of samples at time intervals that can be precisely determined—essential for meaningful data in digital signal processing systems, where sampling must occur at known (and almost always uniform) rates. The sampling, digitization, and processor *read* operation can occur at rates up to 50 kHz, suitable for signals containing frequencies up to the Nyquist limit of 25 kHz.

With a single +5-volt supply, the differential inputs accept both unipolar and bipolar signals (0 to +2.5V, 0 to +5V, and ±2.5V). Besides the input and power, the only other externality required is a 2.5-volt reference (plus clock and control signals). The AD7579, designed for 8-bit buses, provides an (8+2)-bit multiplexed output format; the AD7579, intended for wider busses, has a 10-bit parallel output. Otherwise, the converters are essentially identical in function and performance, with microprocessor-compatible high-speed data bus (50-ns *read* pulse) operation.

Besides such traditional static specifications as linearity and offset, these devices also meet a set of dynamic (ac) specifications: signal-to-noise (log) ratio (SNR), total harmonic distortion (THD), and intermodulation distortion (IMD). These specs are especially meaningful because the sample-hold amplifier, a key element in evaluating dynamic performance, is on-chip; its performance is inherently part of the overall transfer function.

With all these features, the inherent virtues of linear-compatible CMOS (LC²MOS)—small size and low power consumption (less than 50 mW at +5 V)—are maintained. The user can choose

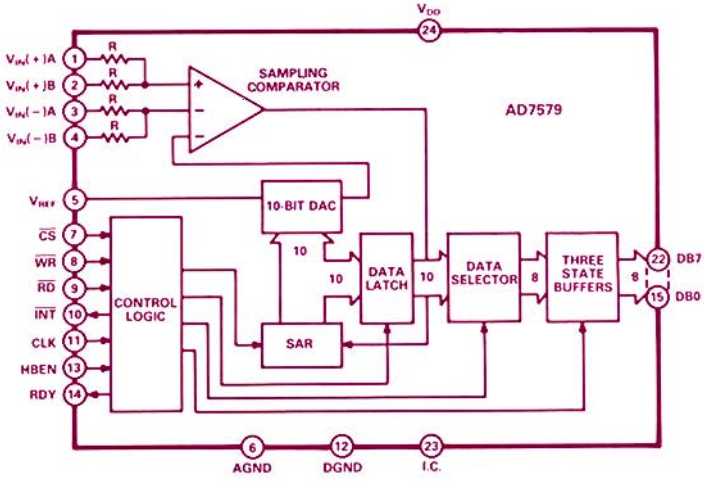
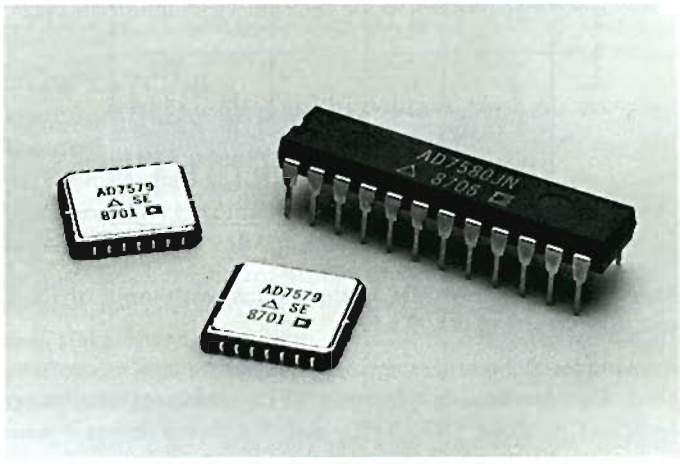


Figure 1. Block diagram of the AD7580. The AD7579 has the same functions, but the 10-bit-wide digital interface is replaced by a multiplexed 8-bit interface.

*Use the reply card for technical data.



0.3"-wide 24-pin "skinny" DIP (plastic or hermetic) packages—or plastic or ceramic chip carriers for surface mounting. Prices begin at $9.00 (100s).

OPERATION OF THE AD7579/AD7580

Input circuitry. The block diagram, Figure 1, shows the differential input circuitry used for input signal flexibility. Instead of a single-ended input referred to analog ground, there is a pair of differential inputs. They can operate over a wide common-mode voltage range, and direct differential measurements may be made. This is useful if the signal source has a remote ground at a different potential from the ADC ground, or if signals are used that are not directly ground-referenced (such as from bridge-type transducers). Of course, single-ended positive ground-referenced signals can also be measured. The built-in input resistors can be configured as attenuators to scale and offset the analog input voltage; they track with better than 10-bit accuracy.

Sample-Hold. When an ADC is used to digitize a signal, the signal applied to the conversion circuitry must not change by more than ½ LSB during the conversion process. This limits the bandwidth a converter can normally accept. The sample-hold circuit of the AD7579 and AD7580 "freezes" the input signal to the converter during the conversion process, and allows wider-bandwidth signals to be accepted. The sample-hold function is inherent in the converter's charge-balancing comparator. It samples the difference between the high and low input voltages and compares this voltage against the DAC's output during conversion. The proven capacitor-coupled "sampled-data" comparator design can also be found in such ADCs as the AD7575, AD7576, and AD782X series.

Converter and Clock. The a/d conversion is realized with a 10-bit DAC and a successive-approximation register. An external clock, normally operating at 2.5MHz, drives the conversion process. Specified linearity is maintained for clock rates from 250 kHz to 2.5 MHz, with a (typical) doubling of error at 50 kHz due to leakage effects of the s-h circuit's *hold* capacitor. With the 2.5-MHz clock, the maximum conversion time is 18.5 μs; with 1.5 μs added

for reading the data outputs, the total conversion cycle is 20 µs (50 kHz). A 2.5-V reference, such as the Analog Devices AD580, is required for the DAC; a trimmable reference permits the full-scale error, specified at ± ½ LSB max, to be trimmed out.

Digital Interface. A conversion cycle begins after the chip is selected and $\overline{WR}$ (Write) goes *low*; this sets up the internal logic. When $\overline{WR}$ returns *high*, the actual successive-approximation conversion is started. The result of the conversion process is transferred to a three-state output latch, and a flag-bit interrupt is set—signalling to the processor that conversion is complete and new data is available to be read. A processor *read* cycle, using $\overline{CS}$ and $\overline{RD}$ lines, allows the data to be accessed in a single cycle for the AD7580. For the 8-bit-output AD7579, two *reads* are used; an extra control line allows the processor to access either the 8 LSBs or the 2 MSBs of the 10-bit conversion during a *read* cycle.

DYNAMIC PERFORMANCE SPECIFICATIONS

In digital signal-processing (DSP) applications, where the result of the analog-to-digital conversion will be used in extensive calculations—such as for pattern recognition, FFTs, echo cancellation, and adaptive filtering—the standard dc (static) specifications of linearity error (both differential and integral) and offset error are not sufficiently informative. The function of an ADC is to provide an accurate digital representation of the instantaneous amplitude of the changing input signal at precisely determined intervals. Besides the inherent quantization (roundoff) error due to the limited number of bits, variations in sample times (jitter) or errors in conversion can produce significant errors after the repeated numerical operations that DSP algorithms require; errors may even grow appreciably on each cycle of calculation.

Differences between ideal performance and real converter dynamic performance are due to bandwidth, settling time, and slew-rate limitations within the converter, as well as time jitter (uncertainty caused by propagation variations in the conversion timing signals and sample-hold circuitry). Dynamic testing is usually done with high-purity sine-wave inputs; they are used because sine waves are reproducible using available equipment, they can be described and analyzed fully, and the relationship between sine waves and their numerical analysis after conversion is well understood.

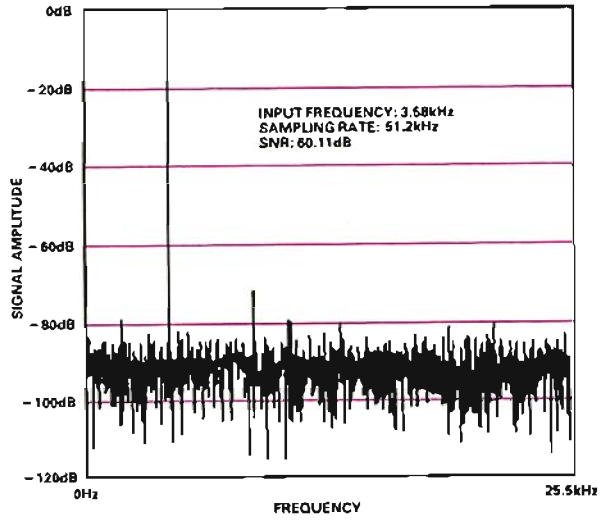


Figure 2. FFT Spectral Response of the AD7579/AD7580.

To meet the needs of these DSP applications, the AD7579 and AD7580 are fully characterized for AC parameters including signal-to-noise ratio (55 dB min), total harmonic distortion (−58 dB max), and intermodulation distortion (typically −67 dB).

Figure 2 shows a 2,048-point FFT spectral response for an input signal of 3.58-kHz (f_0) sampled at 51.2 kHz. The SNR is defined as the ratio of the rms magnitude of the fundamental (f_0) to the rms sum of all non-fundamental signals up to half the sampling frequency. The measured SNR is 60.1dB, with the largest harmonic ($2f_0$) 70dB below the fundamental, while the harmonics above $2f_0$ are barely distinguishable from the noise floor. The theoretical SNR of an ADC is related to its resolution by:

$$SNR = (6.02N + 1.76)\,dB$$

where N is the number of conversion bits, so the measured SNR of the device under test is close to the theoretical 62-dB maximum for a 10-bit ADC. Alternatively, the number of effective bits is determined by using the actual SNR and solving the equation for N; at 9.7, in this case, it is quite near the ideal value of 10 bits.

In order to study the specifics of the nonlinearities, it is useful to look at the distribution of output codes. A histogram, Figure 3, shows the frequency of occurrence of each of the possible 1,024 codes when several hundred thousand samples are taken. For perfect conversions on a sine wave of peak amplitude, A, the probability density function, p(V), would produce the U-shaped relationship:

$$p(V) = \frac{1}{\pi\sqrt{(A^2 - V^2)}}$$

as a function of voltage, V. If a particular step of the conversion is wider than the ideal, the code associated with that step will accumulate more countsthan ideal; a narrower step will have fewer counts, and a missing code will have 0 counts. In this example, measured near the Nyquist frequency, there are no missing codes; the absence of large spikes indicates little differential nonlinearity.

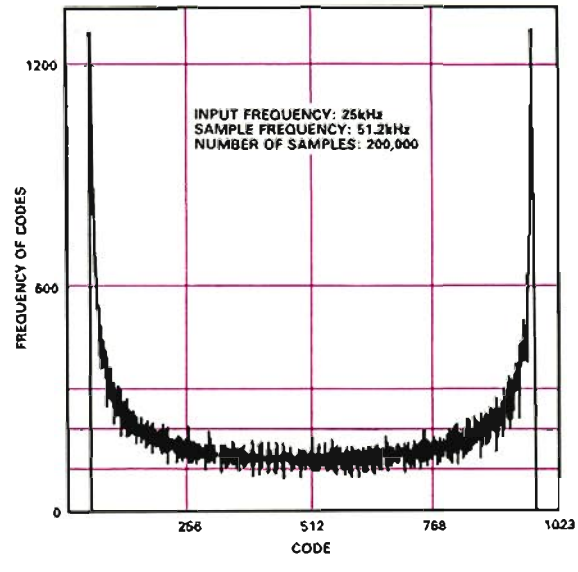


Figure 3. Histogram plot showing frequency of occurrence for each ADC output code.

MONOLITHIC DAC COMBINES SPEED AND ACCURACY

AD568 Has 35-Nanosecond Settling Time, 12-Bit Accuracy Fits into a 0.3"-Wide 24-Pin Cerdip Package

by Pauline Liu

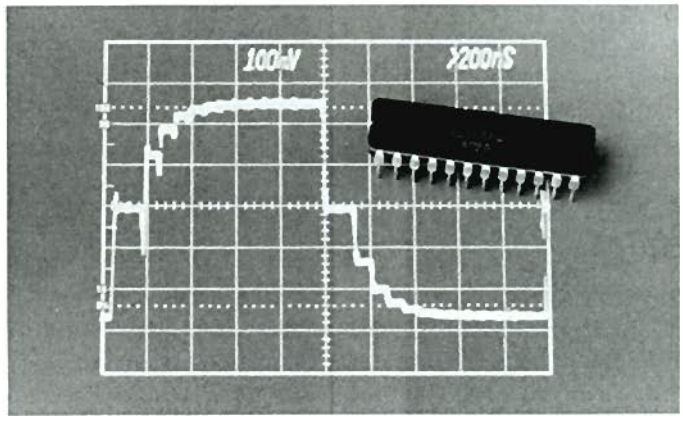
The AD568* (Figure 1) is a fast-settling monolithic 12-bit digital-to-analog converter housed in a 0.3"-wide cerdip package. Employing a proprietary complementary-bipolar process—for combined speed and accuracy—it contains a current-output d/a converter, a buried-Zener diode reference, and application resistors for scaling its voltage output, either passively or via an external operational amplifier.

Its output typically settles in 35 nanoseconds to within ±0.025% of full-scale current (50 ns for voltage). Despite this fast performance, accuracy is not sacrificed: maximum differential nonlinearity is ±1 LSB, ensuring monotonicity over the specified temperature ranges. Typical applications are as a building-block of high-speed, high-resolution a/d converters, as a high-speed, high-accuracy component of vector-graphic displays, and in direct digital frequency synthesis.

Its full-scale output current is 10.24 mA (2.5 μA per bit); matched on-chip resistors and a bipolar-offset-current source provide selectable full-scale output voltage ranges of 0 to 1.024 V and ±0.512 V (250 μV/bit). An on-chip 1-kΩ span resistor facilitates a buffered 10.24-volt output span, when used as the feedback resistor of an external buffer op amp or track-hold.

Three grades are specified over two operating temperature ranges: 0° to +70°C for the JQ and KQ grades, and −55°C to +125°C for the SQ grade and its 883B versions. The JQ and SQ grades specify a ±3/4-LSB maximum integral-linearity error over temperature; the KQ grade guarantees a maximum of ±½ LSB. Maximum differential nonlinearity is ±1 LSB for all grades; maximum voltage-gain drift is ±30 ppm/°C for KQ and ±50 ppm/°C for the other grades. Maximum full-scale current drift is ±150 ppm/°C for all grades. The AD568 will operate at supply voltages from ±13.5 V to ±16.5 V; it typically dissipates 525 mW. Prices start at $35 in 100s.

Applications. The AD568 is useful for applications where 12-bit resolution and accuracy, maintained over the operating temperature range, must be combined with fast settling. Typical applications include the design and construction of submicrosecond high-resolution a/d converters (both successive-approximation and subranging), setting gains in analog circuitry with high speed and precision, and upgrading the speed capability of systems originally designed to use internally referenced 12-bit current-output d/a converters, such as the AD565A. Figure 2 shows the basic analog connections for obtaining −1.024-volt full-scale output.



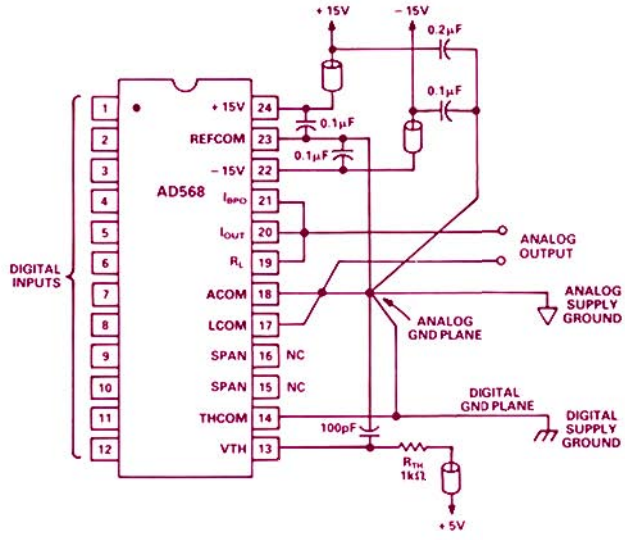


Figure 2. Basic connections for ±1.024-volt full-scale output.

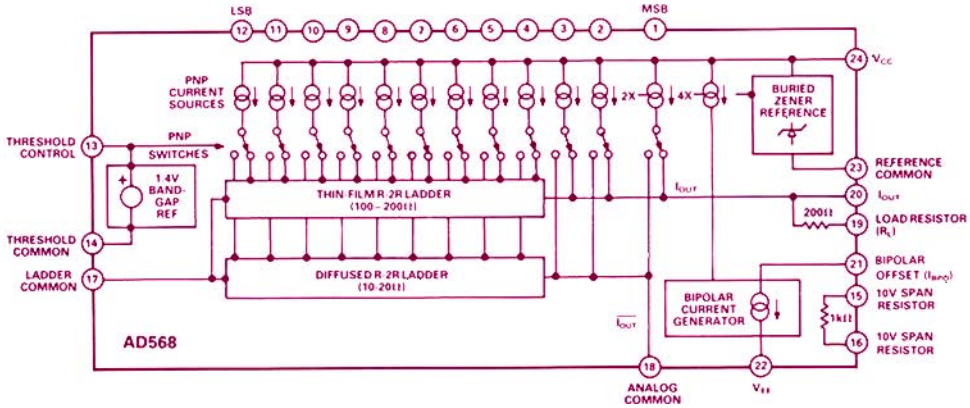


Figure 1. Block diagram of the AD568.

*Use the reply card for technical data.

22-BIT COMPLETE MODULAR INTEGRATING A/D CONVERTER

AD1175 Performs 20 Conversions per Second, Is µP-Compatible

Maximum Integral Nonlinearity is ½ ppm of Span

by Geoff Haigh and Bill Sheppard

The AD1175K* is a 21-bit-plus-sign microprocessor-compatible analog-to-digital converter housed in a 3.7" × 5.2" × 0.53" metal case. An integrating-type converter with high noise immunity, it performs 20 conversions per second in 60-Hz environments (16-per-second @ 50 Hz).

Intended for applications that require the highest possible accuracy, it provides the performance of large benchtop or rack-mount instruments in a compact, modular package without sacrificing conversion speed, board space, or economy (its price is only $495 in 100s—$795 in small quantity).

WHAT IS IT?

The AD1175 (Figure 1) contains a complete microcomputer-based measurement subsystem and can be interfaced to any microprocessor-based system via an 8-bit data bus. Simple bus commands initiate conversions, control the adjustment of offset and coarse gain, and provide nulling for external offsets. The offset and gain settings can be stored to nonvolatile memory upon command.

Small enough to mount directly on an IBM PC card, the AD1175 can be operated *inside a personal computer* as part of a high-accuracy data-acquisition system and/or a 6½-digit DVM with little if any reduction in performance. A scheme that accomplishes this successfully can be found in Figure 4.

Key performance aspects include 22-bit resolution (21 bits plus sign) and 133-dB dynamic range, ± ½ ppm *max* integral nonlinearity over the input span (± 1 ppm *max* from 0 V to ± full-scale), ± ½ LSB *max* differential nonlinearity, and low temperature coefficients: 0.5 µV/°C max for zero and 1 ppm/°C max for gain.

Typical applications include scientific and medical instruments, ATE, weighing systems, data acquisition, and test/measurement equipment. It can be used instead of much larger and more costly

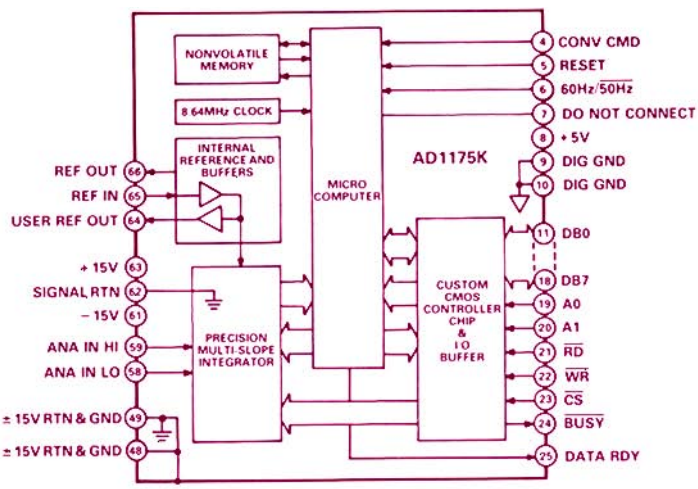


Figure 1. Block diagram and connections of the AD1175.

*Use the reply card for technical data.

conversion "boxes"; it can also obviate the need for user-designed-and-built devices where compactness and low production cost are of primary importance.

HOW IT WORKS

The AD1175 is a complete a/d converter, consisting of three major elements: a linearized auto-zeroed integrator, a single-chip microcomputer, and a custom CMOS controller/bus interface chip. Figure 2 shows the functions within the AD1175 that contribute to its resolution, accuracy, and versatility. An *integrating* converter, it is a member of the family that includes v/f converters, dual-slope converters, and charge-balance converters. The common feature of all of these is the use of *time* (which can be resolved and measured very accurately) to measure voltage, by the equating of charge during a reference period and a measurement period, viz.,

$$\Delta \text{ Charge in} = \Delta \text{ Charge out}$$

where Δ Charge (Δq) is

$$\Delta q = \int_0^T I\,dt = \int_0^T \frac{V}{R}\,dt$$

For an integrating converter, conditions are adjusted so that the Δq developed by integrating the current produced by a reference voltage (V_{ref}) applied across a measuring resistor (R_{int}) for an interval, T_{ref}, is equal to the Δq when a signal voltage (V_{sig}) is applied to the same resistor for a period, T_{sig}:

$$\frac{1}{R_{int}} \int_0^{T_{sig}} V_{sig}\,dt = \frac{1}{R_{int}} \int_0^{T_{ref}} V_{ref}\,dt$$

Since V_{ref} is constant,

$$\int_0^{T_{sig}} V_{sig}\,dt = V_{ref} T_{ref}$$

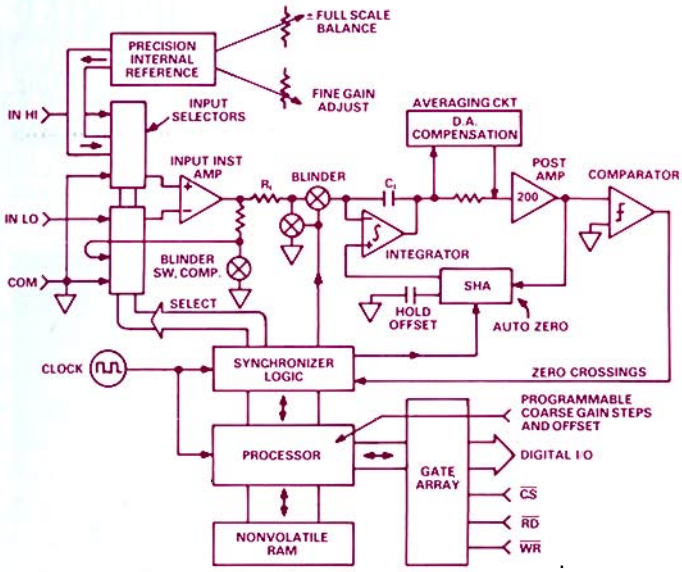


Figure 2. Functions within the AD1175.

Dividing both sides by T_{sig},

$$\frac{1}{T_{sig}}\int_0^{T_{sig}} V_{sig}\,dt = \text{Average}\,(V_{sig}) = \frac{V_{ref}T_{ref}}{T_{sig}}$$

Thus T_{ref}, as a function of the average value of V_{sig}, is:

$$\frac{T_{ref}}{T_{sig}} = \frac{\text{Average}\,(V_{sig})}{V_{ref}}$$

where V_{ref} and T_{sig} are held constant. Paraphrased: the ratio of the average value of the signal measured to the (constant) reference voltage is equal to the ratio of the *measured time* (to force the integrator back to zero charge) to the *signal integration time* (held constant). The implication here is that, since time can be readily resolved to small fractions of a microsecond, very high resolutions can be obtained if the averaging can be performed accurately and error sources either averaged to zero by the end of the conversion cycle or excluded by tricks of timing.

The AD1175's conversion process is somewhat similar to the classical dual-slope technique, where the input signal is integrated over an accurately determined period comprising a whole number of line cycles (for line-noise rejection), and then the time required to drive the integrator back to zero is measured digitally.

In the AD1175, the sequence of integrations is performed 10 times over two cycles of the power-line frequency (33 1/3 ms at 60 Hz or 40 ms at 50 Hz), and a final slow vernier integration (about 6 ms) is performed on the residuals. These readings are summed, the 22-bit numeric result (plus an OVERLOAD bit) is placed in addressable output latches, and data is indicated as available. During the next 10 milliseconds, the integrator is reset; an auto-zero circuit nulls out offset errors in preparation for the next conversion.

The integration intervals are programmed and timed by a high-resolution clock. At any time that no input is supposed to be applied to the integrator, a set of *pause*, or "blinder," switches puts the integrator in *hold* with better than 10-ns resolution.

While the integrator is "blinded" to the input circuitry, inputs can be switched (e.g., between signal and reference) without introducing errors. In this state, the integrator is auto-zeroed once per measurement cycle, using a loop with a gain of 300 million; a sample-hold measures the offset, *holds* it, and feeds it back to the input as a correction during the next cycle. Because there are between 10 and 20 corrections per second, they greatly reduce the effects of classic 1/f noise in the 0.1 to 10 Hz range, as well as thermal drifts. Errors that might be introduced by the switches themselves are compensated for by introducing a compensating error in the *low* side of the input circuitry.

INTERFACING

While extreme caution is always necessary in making 22-bit measurements, the AD1175's shielding and design for insensitivity to noisy environments, as well as its interfacing capabilities, tend to make it a friendly helper to the measurement engineer.

The AD1175 interfaces to any microprocessor-based system in either a memory- or I/O-mapped mode via an 8-bit bidirectional data bus and its associated control lines. The output consists of 4 addressable 8-bit bytes (3 data bytes + *Status*), which indicate magnitude, polarity, offscale condition, and additional status information. Bus commands initiate conversions and control *offset adjust*, *coarse gain adjust*, and an external offset null feature. Internal nonvolatile memory stores offset and gain settings on command. User-accessible trim potentiometers adjust fine gain and ± full-scale balance.

The analog input is a high-impedance, high common-mode-rejection, true-differential input pair; input *low* senses the low side of the signal at the source to minimize ground-loop problems. The nominal ±5-volt full-scale input range is adjustable from ±4.7 volts to ±5.6 volts, but rated accuracy is specified for inputs up to 10% over normal (for a total dynamic range greater than 4.6 million : 1).

Power supply requirements are ±15V dc and +5V dc. No external components are needed for operation to specified performance; integration time is user pin-selectable for maximum line-frequency noise rejection at either 60 Hz or 50 Hz. All digital input/output lines are LSTTL compatible.

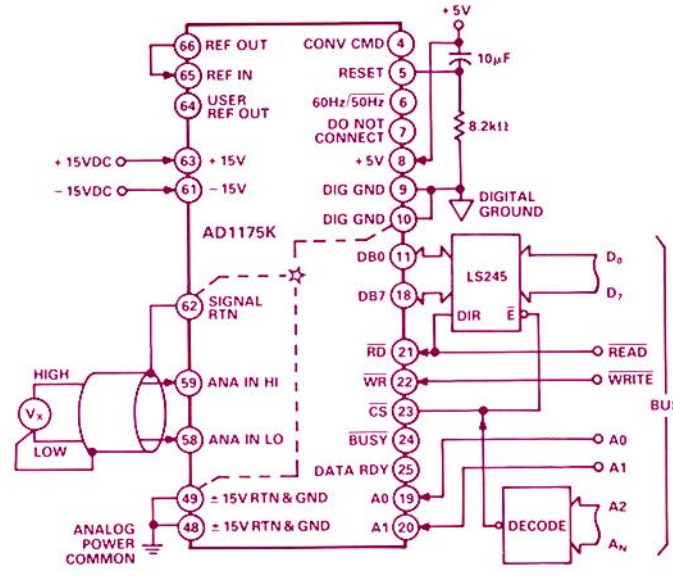


Figure 3. Interfacing to a bus—basic connection.

The 6.95 V (±2%) reference provided in the AD1175 is temperature controlled for stability to within ±0.8 ppm/°C and has a long-term stability to 25 ppm/1,000 hours, maximum, after 15 days of operation. Its output is jumpered externally to the REF IN terminal; this makes it possible for an external reference to be used, or for the AD1175 to be operated ratiometrically. A buffered version of the high-stability internal reference is available for other user purposes.

Figure 3 illustrates a typical set of connections to the AD1175. The ANA IN LO pin provides remote sensing of the low side of the input with high common-mode rejection. Since it is an instrumentation amplifier, the voltage at ANA IN LO can and will differ from that at SIGNAL RTN, but—not being isolated—they should be kept within ±100 mV of one another; for similar reasons, galvanic paths from both inputs to SIGNAL RTN are needed as bias-current returns.

I/O FOR IBM PC BUS

In order to see how the AD1175 operates in a noisy and hostile digital environment, we built an experimental data-acquisition board designed to be plugged into one of the accessory sockets of an IBM PC/XT computer (Figure 4).*

There are four multiplexed differential-input channels, with input characteristics similar to those of the AD1175 itself. One of them could be used for remote ground sensing (i.e., HI, LO, and remote ground tied together at the remote location), providing a system-offset measurement for the other three channels. Power is provided from the +5-volt computer power bus via a Model 949 dc-to-dc converter; additional power during initial heating of the internal reference oven is provided from the PC's ±12-volt power supply via a pair of diodes.

To be sure of adequate drive capability, the bus is buffered by U3, a 74LS245. The I/O address space of the PC is decoded by U4, a 74LS688; I/O decoding starts at address 300_H. Latch U2 stores the address of the chosen input of MUX U1. U5 decodes the I/O address for the latch and an I/O address dedicated to the resetting of the AD1175 via U6, used as a Reset pulse generator.

A set of benchmark measurements compared performance of an AD1175 mounted on the prototype card operating inside the PC with that obtained in bench operation under ideal conditions. *No discernible difference was observed in the AD1175's performance, except for an additional ½-code of peak-to-peak noise near full scale* and about 20 μV of additional warmup offset due to thermocouple effects at the terminal strip protruding through an I/O slot opening at the rear panel of the PC.

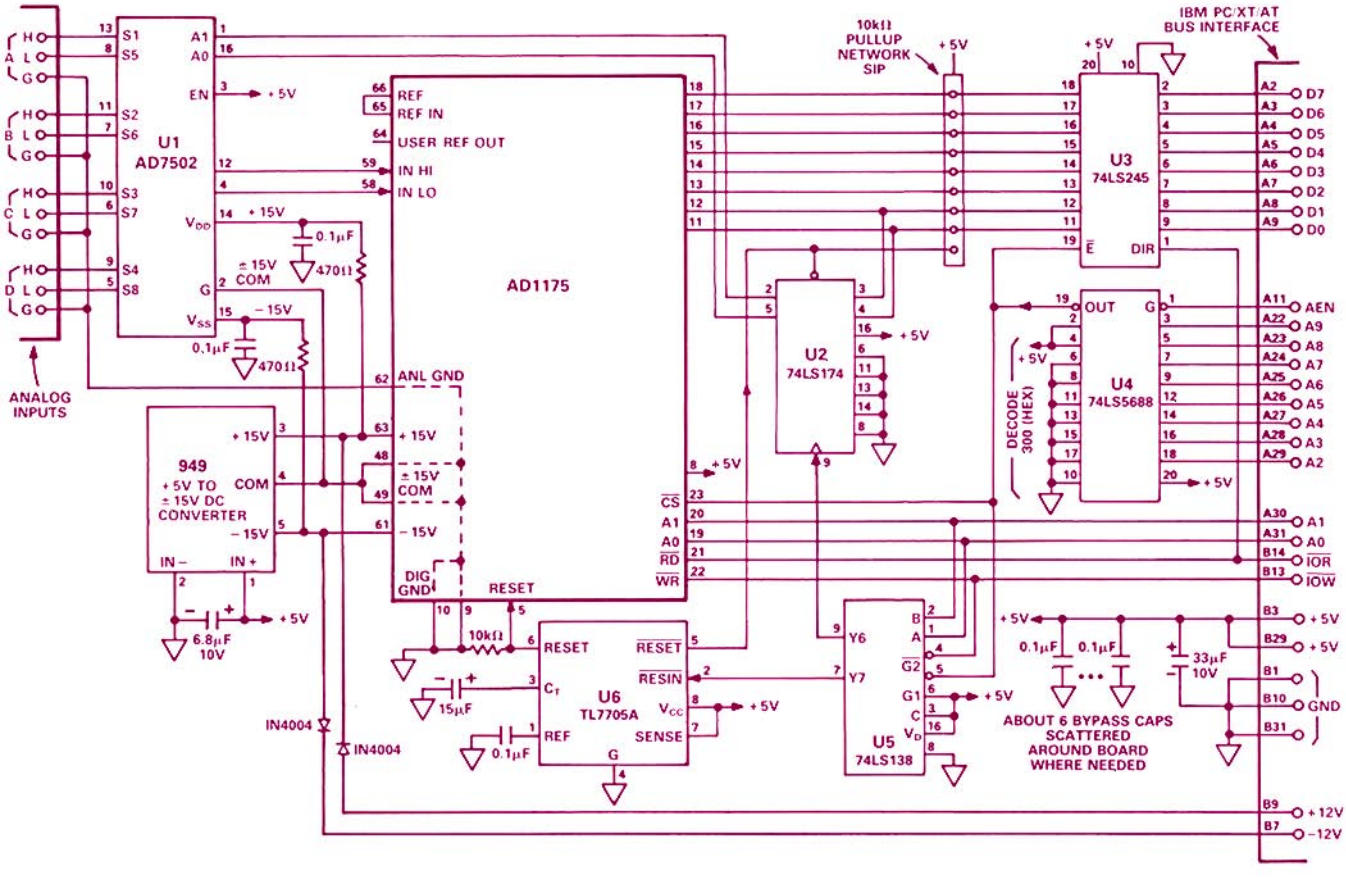


Figure 4. Interfacing to the IBM PC/XT/AT.

*Use the reply card for an Application Note describing this circuit in greater detail and including many practical suggestions.

MONOLITHIC SOFTWARE-PROGRAMMABLE-GAIN AMPLIFIER

AD526 Has Gains of 1, 2, 4, 8, 16—Cascadable to 32, 64, 128, 256
Use It for Range Extension, Floating-Point A/D Conversions

by John Krehbiel

The AD526* is a complete monolithic software-programmable-gain amplifier (SPGA) housed in a 0.3"-wide 16-pin ceramic DIP. It comprises a FET-input amplifier, resistor network, FET switches, and TTL-compatible input latches (Figure 1). A single AD526 provides binary gain steps from 1 to 16, as established by a single 3-bit gain-control word, W; (Gain = 2^W). Two units can be cascaded for gains up to 256; with the 3-bit control word alone, binary gains from 1 to 128 can be achieved without additional components.

The AD526 is designed for applications calling for programmable gain, dynamic-range extension, and/or floating-point conversion. PGAs of its class are needed for data-acquisition systems that require up to 12-bit resolution and accuracy while dealing with signals having dynamic ranges up to 96 dB. Its high performance and reliability, compactness, and low cost make it preferable to "home-brew" designs, commercially available SPGAs having lesser functionality and performance, and higher-cost hybrids.

PERFORMANCE

For gains of 1, 2, and 4, its gain error (C grade) is less than 0.015% maximum over temperature; it remains less than 0.03% max over temperature for gains of 8 and 16. Nonlinearity over temperature for any grade at any gain >1 is less than 0.001% of full-scale range; for gain = 1, it is less than 0.01%. Input offset voltage is less than 0.7 mV at 25°C—and less than 1.0 mV (0.01% of full scale) over the temperature range for any grade. Bias current at 25°C, fully warmed up, is 150 pA maximum for all grades.

Dynamic response is also excellent. For step input changes, the AD526 has a maximum settling time to 0.01% of final value

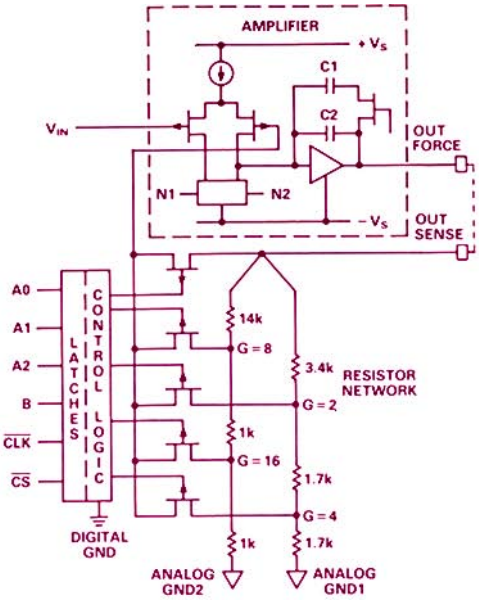
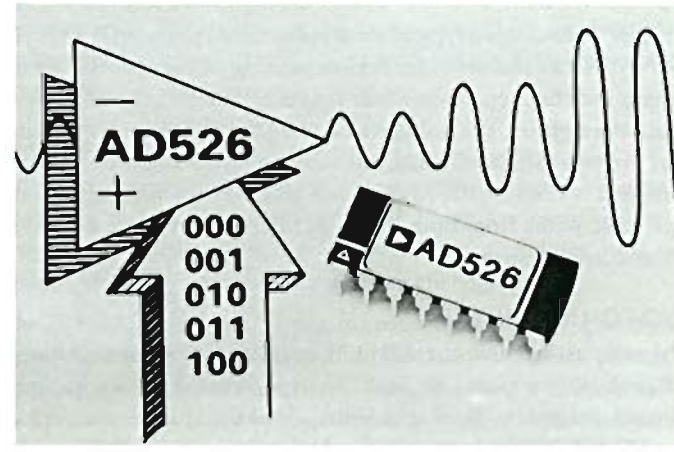


Figure 1. Simplified schematic diagram.



(ΔV_{OUT} = ±10 V) of from 4 to 7 μs, depending on the gain setting. Minimum slew rate is 4 V/μs for gains of 1, 2, and 4—increasing to 18 V/μs for gains of 8 and 16; and full-power bandwidth at gain of 16 is 350 kHz.

The AD526 is available in three performance grades (A/B/C) for operation from −25°C to +85°C—and an "S" grade for operation in the MIL temperature range (−55°C to +125°C); the "S" grade is also available in an 883 version, and a low-priced JN version is now available. Prices (JN grade) start at $5.25 in 100s.

CIRCUITRY & INTERFACING

The AD526's signal path consists essentially of an operational amplifier connected as a follower-with-gain (Figure 1); the circuit's gain is the inverse of the feedback attenuation. A pair of attenuators provides five taps, with attenuations corresponding to the gain values of 1, 2, 4, 8, 16. The 3-digit gain-control code corresponding to a given value of gain causes the appropriate attenuator tap to be connected to the amplifier's feedback input via an FET switch. The on resistance of the switches causes negligible error, since the only current flowing through them is the amplifier's minuscule bias current.

The feedback path between the amplifier output (pin 5, "Force") and the attenuator input (pin 6, "Sense") is closed externally, forming a set of Kelvin connections. The high-impedance Sense pin reads the actual delivered output voltage; it causes the feedback circuit to drive the Force pin to maintain that voltage accurately, irrespective of loading on—or lead resistance in series with—the Force output terminal.

The latches can be connected for either of two modes of operation—transparent and latched. In the *transparent* mode, the gain switches respond directly to level changes at the gain-code inputs; in the *latched* mode, the gain code is stored in the latches under the direction of control inputs $\overline{CLK}$ and $\overline{CS}$. After a change in gain code, the AD526's output voltage typically requires about 5.5 μs to settle to within 0.01% of the final value. Figure 2 shows connections for the latched mode.

Use the reply card for technical data.

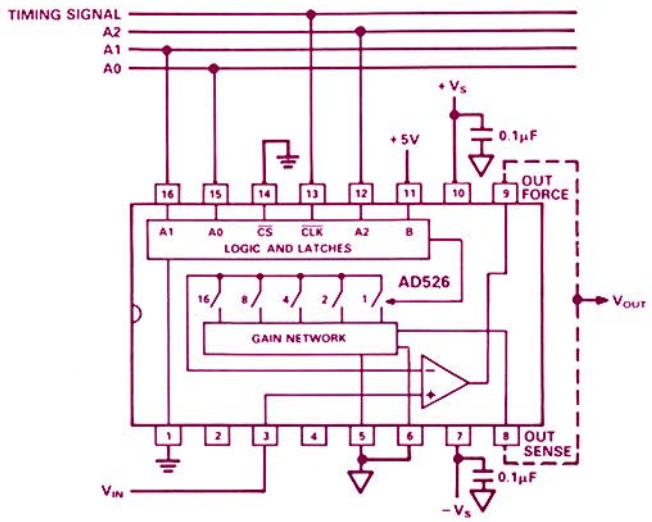


Figure 2. Operation in latched mode.

APPLICATIONS

The AD526 is useful in applications calling for 12-bit accuracy with dynamic ranges up to and beyond 96 dB. A typical application is in the design of floating-point a/d converters. The AD526 is the key to design of a floating-point converter having a 12-bit mantissa and a 3-bit exponent.

In the circuit of Figure 3, the input is sampled (AD585) and applied to a set of comparators; it is compared against a sequence of scaled voltages (based on an AD588 precision reference) to determine the amount of gain needed to scale the input signal to a range between half scale and full scale. The comparator outputs are priority-encoded into a 3-bit gain-control word—in a manner very much like a "flash" converter (in fact, the comparators and encoder serve as an exponential flash converter). The gain-control word also serves as the leading three bits of the output.

The sampled input is applied to the AD526; its output is sampled and converted, using a fast 12-bit a/d converter (AD7572). Since there are two sample-holds, the system is pipelined; i.e., while a sample is being held by the second sample-hold and converted—and its exponent remains latched—the gain-control word for the next sample is being determined and becomes ready for latching; meanwhile, the signal is amplified into the normal range and settles to its final value. Then the second sample-hold goes into Hold, its output is converted, and its exponent is latched.

The acquisition time for the AD585 is 3 µs, and the conversion time of the AD7572 is 5 µs, so a new conversion can be performed at intervals of about 8 microseconds—a rate of about 125 kHz. The dynamic range of this circuit (the log ratio of full-scale to the value of 1 least-significant bit) is 96 dB; in these circuits, the value of the extended-range LSB is the ratio of the value of the 12-bit LSB to the maximum gain of the PGA. ◘

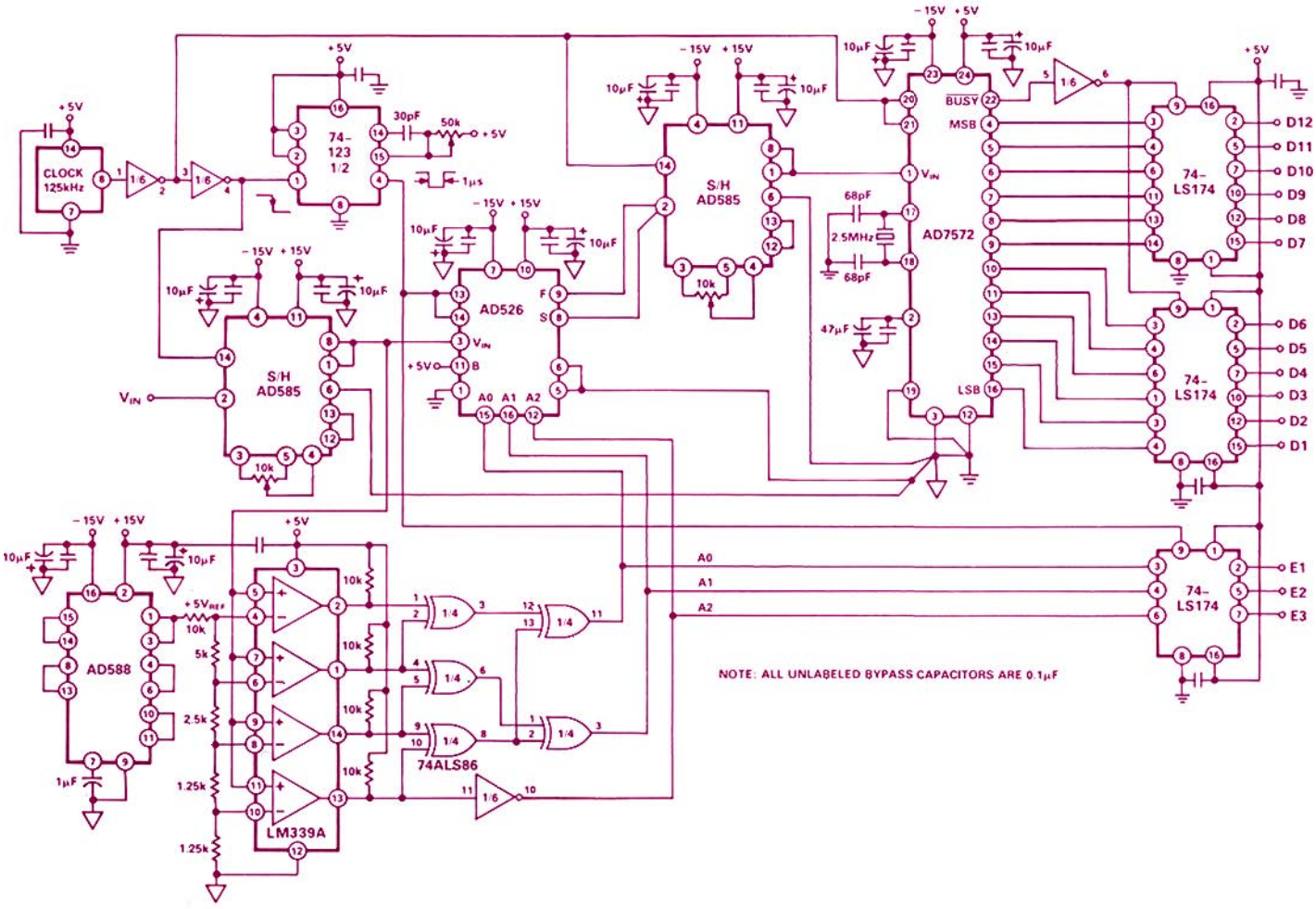


Figure 3. Floating-point a/d converter.

FAST, ACCURATE BiFET OP AMP SETTLES TO 0.01% IN 900 ns MAX

AD744C Slews at 75 V/μs, Has 0.0003% Total Harmonic Distortion

Offset is 250 μV max, with 3 μV/°C max Drift and 50 pA max I_b

by Kristin Dinsmore

Op-amp users have often had to compromise between the desired ac performance characteristics: short settling time, fast slew rate, minimal overshoot and ringing; the required dc specifications: minimal offset voltage, drift with temperature, and input bias current; and low power consumption. This technical trade off is now made much less of a dilemma: the AD744* op amp uses BiFET technology, innovative design, laser trimming, and ion-implanted JFETs to achieve outstanding ac *and* dc performance in a monolithic device.

The design of the AD744 results in fast settling time, with minimal ringing. Critical specifications are either assured by design or 100% tested, so that the designer can work with both typical and "worst-case" values in the analysis of the application. For a 10-volt input step, the output will typically settle to within 0.01% in 500 nanoseconds; the maximum settling time is 900 ns. The slew rate is tested to be at least 50 V/μs, with a typical value of 75 V/μs. User-selected optional compensation enables the op amp to drive capacitive loads greater than 2,000 pF with full stability; a slew rate of 10 V/μs can be achieved with a 1,000-pF load.

Fast response does not mean that dc precision is sacrificed. 100% of the devices are tested for maximum voltage offset less than 250 μV and drift less than 3 μV/°C. Warmed-up input bias current, guaranteed less than 50 pA for the best grade of the AD744, is typically about half that figure. Noise in the 0.1-to-10-Hz band is below 4 μV peak-to-peak, and open loop gain is at least 250,000.

The combination of these specifications makes the AD744 ideal for buffering d/a and a/d converters in 12-, 14-, and 16-bit systems, driving cables, wideband preamplification, and active filtering. Demanding audio designs can benefit from the very low total harmonic distortion (THD) of only 0.0003% and gain-bandwidth product (GBW) of 13MHz. For DSP mixed-signal applications, this op amp is an excellent ac preamp because the GBW can be extended to beyond 200MHz at high gains with external decompensation.

The AD744 is available in hermetic 8-pin CERDIPs and TO-99 cans, as well as plastic mini-DIPs. A power supply of ±4.5 V to

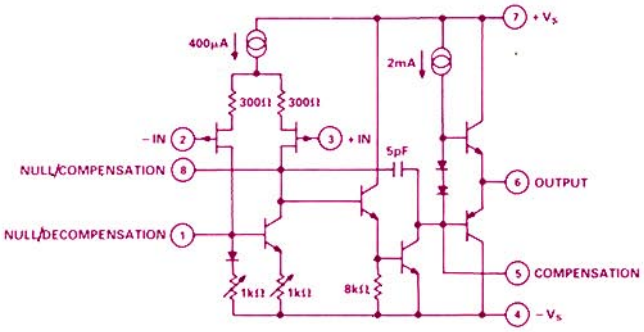
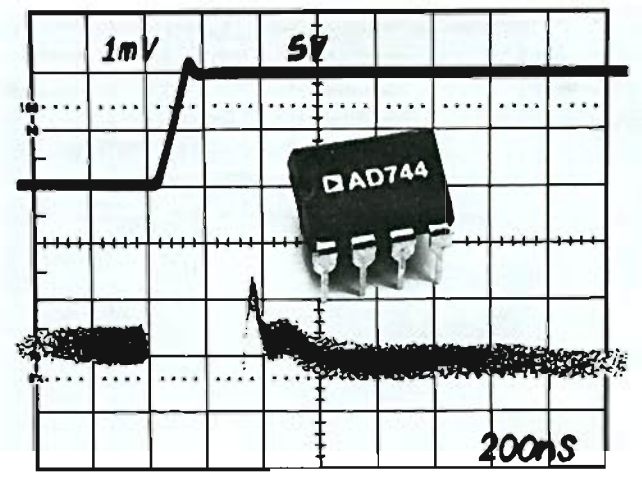


Figure 1. The simplified schematic of the AD744 shows the relatively simple two-stage architecture.

*Use the reply card for technical data.



±18 V is required; the quiescent current is typically 3.5 mA, 5 mA maximum. Operating temperature ranges span 0 to +70°C, −40°C to +85°C, and −55°C to +125°C depending on grade; processing to MIL-STD-883 and devices in chip form are also available. Pricing ranges from $2.25 to $7.95 (100's).

A simplified schematic of the AD744 is shown in Figure 1. The relatively simple two-stage architecture with compensation approximates a single-pole response and provides excellent dynamic performance. The result is seen in Figure 2, as the clean, sharp half-μs 0.01% settling response to full-scale positive and negative square waves. The low noise level: 16 $nV/\sqrt{Hz}$, or a total of 58 μV rms (0.4 mV p-p) over a 13-MHz bandwidth suggests the possibility of useful performance in systems approaching 16-bit resolution.

Many monolithic FET-input op amps develop sharply increasing bias current as a function of increasingly positive common-mode voltage, usually forming a "knee" between 0 and +5 volts, due to excess gate leakage current. The process used for fabricating the AD744 virtually eliminates the excess gate current due to impact ionization; the result is that input bias current varies by less than two to one—from 22 to 37 pA, typically—over the entire common-mode voltage range of −10 V to +10 V. This is important for designs such as sample-hold circuits and peak detectors.

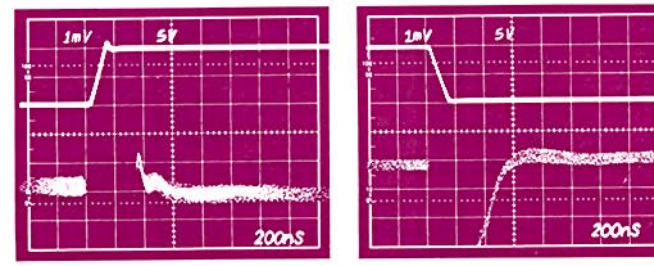
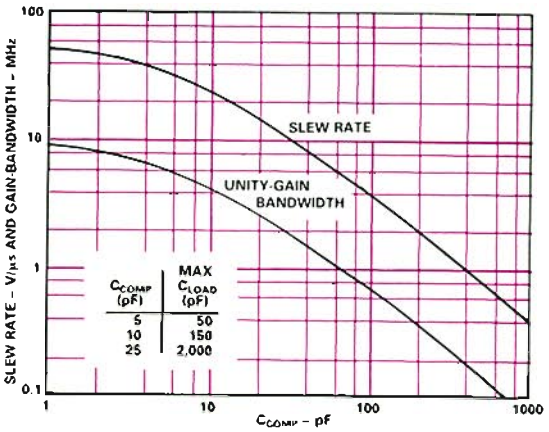


Figure 2. Typical settling time of AD744 as an inverter in response to 0 to +10-volt and 0 to −10-volt square waves (scales: 5 V/div for square wave, 1 mV/div for response, time = 200 ns/div).

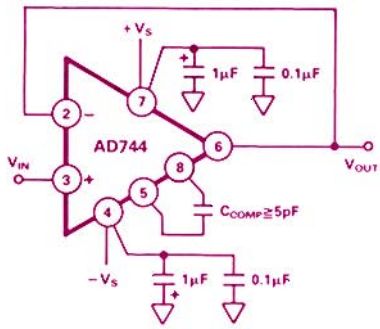
COMPENSATION

The AD744's frequency response is internally compensated, but terminals are provided for optionally increasing *or decreasing* the net compensation. For most applications, including unity-gain inverter and gain-of-two follower, (i.e., applications for which the feedback attenuation, or closed-loop gain ("noise gain") is greater than 2), the AD744 is stable without external compensation.

However, even at gains for which the amplifier is stable only for small capacitive loads, external compensation makes it possible to drive larger capacitive loads stably (Figure 3). A capacitor, C_{COMP}, connected between pins 5 and 8, allows the amplifier to drive loads greater than 2,000 pF, as well as operate at noise gains below 2. The compensation capacitor affects the maximum capacitive load, the slew rate achievable, and the gain-bandwidth product, as shown in Figure 3 for the case of a unity-gain voltage follower. The slew rate and gain-bandwidth product are inversely proportional to the external compensation capacitance.



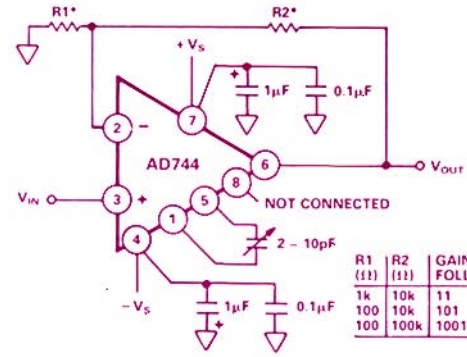
a. Effect of compensation capacitance on unity-gain bandwidth, slew rate, and ability of the AD744 to drive a capacitive load.



b. Compensation circuit for unity-gain follower.

Figure 3. Frequency compensation.

Gain-Bandwidth Product. The uncompensated gain bandwidth product of 13 MHz can be increased for applications where the AD744 is used with closed-loop gains greater than 10, by the use of a small-value decompensating capacitor between pins 1 and 5, as shown in the example of Figure 4. The external capacitance partially nullifies the effects of the internal compensation at low frequencies by applying positive feedback to the input stage. This results in the indicated improvement in gain-bandwidth.



R1 (Ω)	R2 (Ω)	GAIN FOLLOWER	–3dB BANDWIDTH	GAIN·BW PRODUCT
1k	10k	11	2.5MHz	25MHz
100	10k	101	760kHz	76MHz
100	100k	1001	225kHz	225MHz

Figure 4. Extending the gain bandwidth product through the use of an external "decompensation" capacitor, for a noninverting configuration.

APPLICATIONS

An illustrative application is a high-input-impedance, wideband instrumentation amplifier. Three AD744s can be combined to provide a circuit, Figure 5, with gains from 1 to 1,000. At unity gain, the bandwidth is 3.5MHz; it is 1MHz at a gain of 10. The settling time to within 0.01% at a gain of 10 is less than 2 μs for a 10-V step input; slew rate in the positive direction is greater than 30 V/μs. Gain is set by a single resistor, R_G.

If it is necessary for this circuit to operate at gains as low as unity, the phase margin—and therefore stability—can be increased to an acceptable level by using a resistor and a small-value capacitor in parallel between the output and inverting input terminals of the output amplifier. The penalty for this technique is a small reduction in bandwidth at low gains.

As a matter of course, high-speed, wide-bandwidth circuits using high-performance active components, such as the AD744, require adequate bypassing. Each op amp should have a 0.1-μF ceramic capacitor and 1-μF electrolytic capacitor connected from the +V and −V supply rails to the system analog ground, connected as closely as possible to the op amp's terminals.

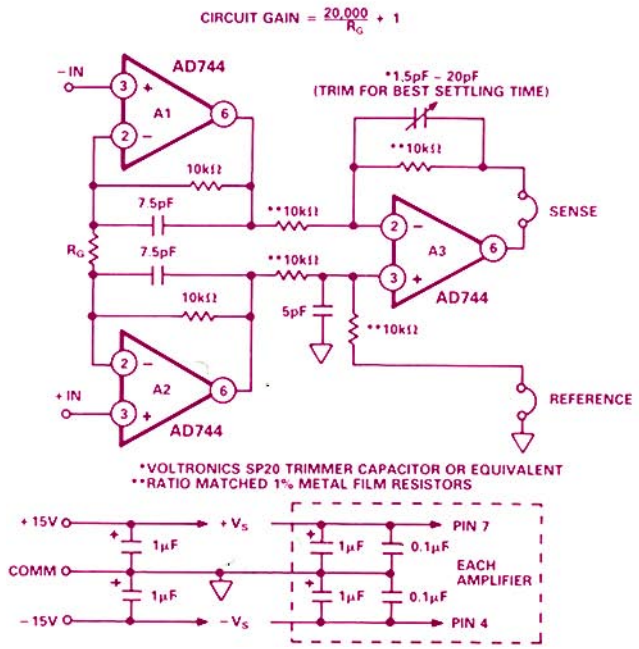


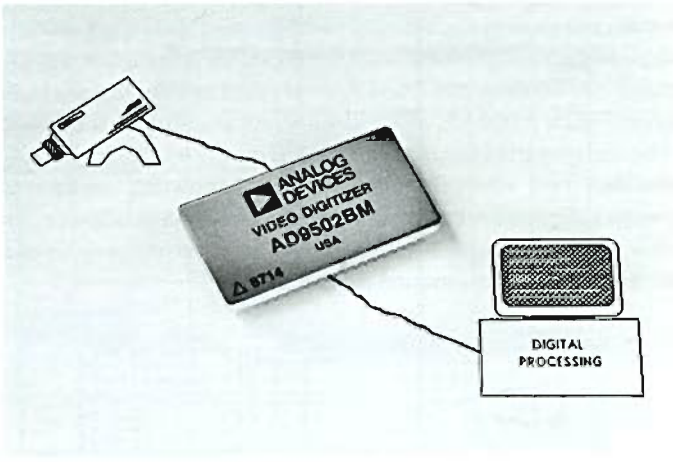
Figure 5. Use of AD744 as a high performance instrumentation amplifier, with gains from 1 to 1,000 set by resistance R_G.

8-BIT VIDEO DIGITIZER FOR CAMERAS INCLUDES CONTROL SIGNALS

AD9502 Is a Complete RS-170 Subsystem in a Single 40-Pin DIP, Includes Video Amp, DC Restore, ADC, Sync Separation, & Clock Generator

by Alan Hansford

The AD9502 Video Digitizer* is designed as a direct link between standard video cameras and image-processing systems. It is the first device available on the market to combine the various analog pre-processing functions for proper digitization of a camera signal—timing, synchronization, and restoration of the dc reference levels—all within a single 40-pin hybrid DIP package. Industry-standard RS-170, NTSC, or PAL camera signals can be interfaced to the system video memory simply and quickly, at low cost. The output of the AD9502 is a stream of 8-bit parallel bytes, which represent the intensity of a video signal on a scale of 256 possible values—along with necessary timing signals to store the data in memory in time-coherent fashion.



The first step in nearly all digital image processing systems is to acquire the analog video signal from the camera, convert it to digital form, and place the resulting bits in an image memory. Since the amount of information in the video signal is high, the required conversion rate is also high. However, it takes much more than a fast A/D converter to transform the camera's output signal into a useful digital equivalent successfully. The video output also contains important timing information that must be used—but not confused with the actual intensity signal.

The raster-scan output of an image from the video camera is a continuous analog signal which represents a line-by-line scan of the picture brightness (Figure 1). Each line is then digitized at individual points called *pixels*—picture (*pix*) *elements*. The number of lines and of pixels/line depends on the prevailing standard. At the beginning of each scan line, timing information is inserted by the camera to provide triggering and permit an adequate horizontal retrace interval. Similar synchronization information is inserted after the last horizontal line is scanned; this identifies the end of the complete frame and allows a long-enough interval for vertical retrace before the next image.

Individual horizontal scan lines occupy most of the time needed for each frame. Each line of composite video has four major sections: the actual video signal level of the image, followed by a "front porch", the horizontal synchronizing pulse, and a "back porch" which also contains a reference signal used in color systems. The amplitude of these signals is scaled in IRE (for Institute of Radio Engineers—which developed the first standards) units; 1 IRE unit is 1% of the black-to-white signal range. The front and back porch intervals are at zero IRE level, which serves as a dc reference for the picture information. The sync signals go to −40 IRE.

In order for the video signal to be extracted properly, with the integrity of the image maintained, some key functions must be performed by the video digitizing circuitry:

- the sync pulses must be detected in the video signal and separated to provide output control signals,
- a pixel clock must be generated locked in phase with the horizontal sync. This is a continuous clock; as a result, digital data is provided by the a/d converter even during blanking and sync intervals,
- the pixel clock, horizontal sync, and vertical sync outputs are provided so that external counter-based circuits can map into memory only those pixels that represent the active video period. Synchronization ensures that pixel locations (in memory) for each pixel on a given horizontal line are aligned with corresponding pixel locations on all other horizontal lines,

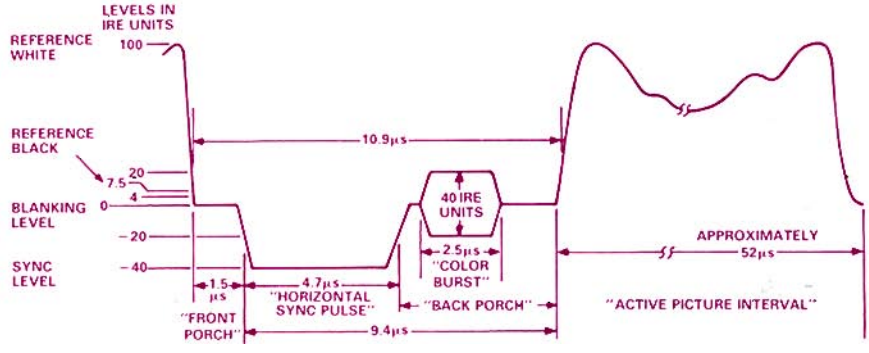


Figure 1. Annotated video signal shows key elements of horizontal timing and intensity standards.

* Use the reply card for technical data.

•the dc reference levels of the video signal must be restored. Although the timing information is extracted by ac coupling, the absolute dc levels contain the picture intensity information.

The appropriate relationship between the vertical sync, horizontal sync, and pixels determines the limits of each image frame.

HOW THE AD9502 WORKS

There are four main subsections used to implement all the required functions: a phase-locked loop (PLL); dc-restoration circuitry; sync detection and timing; and the "flash" analog-to-digital converter. Figure 2 shows a block diagram of the AD9502. All digital outputs are TTL-compatible.

The leading edge of the sync pulse (below the 0 IRE blanking level) is detected and amplified, then used to drive the PLL input as the horizontal sync signal. A vertical sync pulse is generated whenever the incoming sync pulse is longer than 6.6μs. Both vertical and horizontal sync pulses are available to the user, for driving the address counters of the video-data memory.

The PLL has a phase detector, a loop filter and amplifier, a voltage controlled oscillator (VCO), and a digital divider, each fabricated as a monolithic IC. The input to the PLL's phase detector is the train of horizontal sync pulses from the composite video signal, after they have been detected and conditioned. The horizontal sync output is derived from and is similar to this signal. The phase detector generates an output error voltage which is proportional to the difference between the VCO output, divided by N (ratio of pixel clock to horizontal frequency), and the sync pulse rate. This error is the VCO control voltage; if its average value is not zero, it causes the VCO's output frequency and phase to change so as to match the incoming sync signal, thus producing zero error.

Since there is a divide-by-N circuit between the VCO and the phase detector, the closed loop causes the VCO output—the pixel clock—to be N times the horizontal frequency of the input. N is an integer, set at the factory; it corresponds to the desired number of pixels/line, thus defining the picture's nominal resolution. When there is an input signal and the PLL is properly tracking it, the loop is in a "locked" condition; with no input, or while the VCO is hunting and trying to synchronize, it is unlocked.

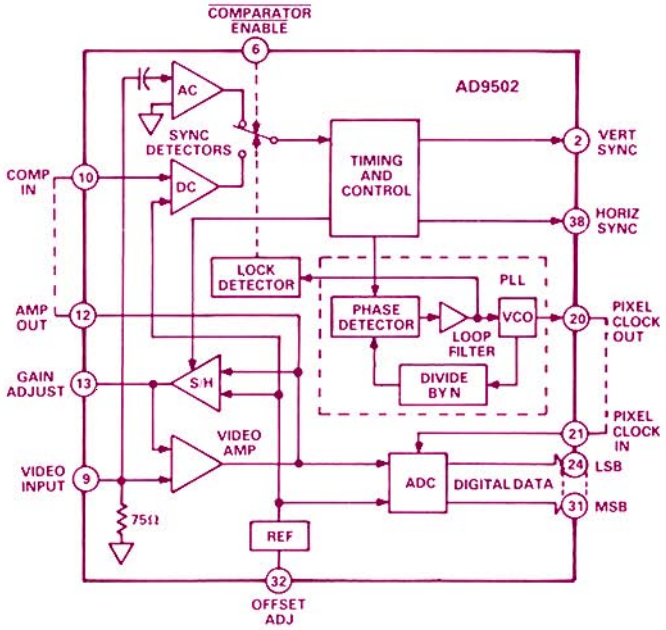


Figure 2. Functional block diagram of the AD9502.

The dc reference level is restored by a sample-hold (S/H) circuit, which samples the input signal after each horizontal sync pulse. During the active-picture-information portion of the composite input signal, the S/H is in the Hold mode and has a constant output. This output is added to the input video signal at the input amplifier, offsetting the input appropriately.

The A/D converter uses the "flash" architecture with a column of comparators at precisely spaced voltages, followed by encoders—which ascertain the correct digital value. The video signal is resolved to 8 bits, with conversion rates up to 13 MHz; the exact conversion rate needed depends on the number of lines per frame, pixels/line, and frames/second. The video signal has a nominal value of 1-V peak-to-peak under the RS-170 standard, but some variation is tolerated in the amplitude and dc offset of the camera outputs. The AD9502 can be compensated for these variations with external adjustments; the gain can be varied by 13 dB and the offset by up to 200 mV.

Although the RS-170 line and frame rates are standard throughout the Western Hemisphere, other rates are important in video use; they include NTSC (National Television Standards Committee) and PAL (used in Europe), as well as those used in hard-wired stand-alone computer applications—which do not involve broadcast receivers. Within each standard line rate, there are variations for the number of pixels/line, which determines the a/d conversion rate needed. Only three models of the AD9502 with overlapping capabilities are needed to support a wide variety of line rates and pixels/line; the reason is that the PLL is designed to adapt automatically to reasonable variations around the nominal setting. A special high-resolution model supports 512 lines × 512 pixels/line, common in computer-vision applications.

EXTERNAL CLOCK DRIVES

Some applications require that multiple cameras be precisely synchronized so that images can be switched, overlapped, or merged. Physical positioning analysis requires very close registration between the camera pixel data and the digitized data, without even the slight jitter that may be tolerated by the PLL. To achieve this, the AD9502 allows an external pixel clock to be used with the VCO disabled; the external pixel clock then controls all conversion cycles. A master sync signal from the master camera or control unit provides horizontal and vertical timing outputs.

The external clock drive is also used where camera output represents color information by red, green, and blue signals; three AD9502s are used. Usually, the "green" device (containing sync) is configured for normal operation; its clock outputs are used to drive the red and blue devices, set up for external clock drive.

The AD9502 provides, in a single package, the complete and complex circuitry needed to provide meaningful digital signals from various video signal formats. Designed to operate over the −25°C to +85°C range, it is available in a 40-pin metal package and requires ±12 to ±15-volt and +5-volt supplies; typical power dissipation is 1.75W. Single-quantity price is $289.

PLUG-IN BOARDS ADD POWER & VERSATILITY FOR VMEBUS USERS

RTI-681-HS Graphics & Video Controller Displays any 256 Colors

RTI-680-HS Array Processor Operates at Video Rates

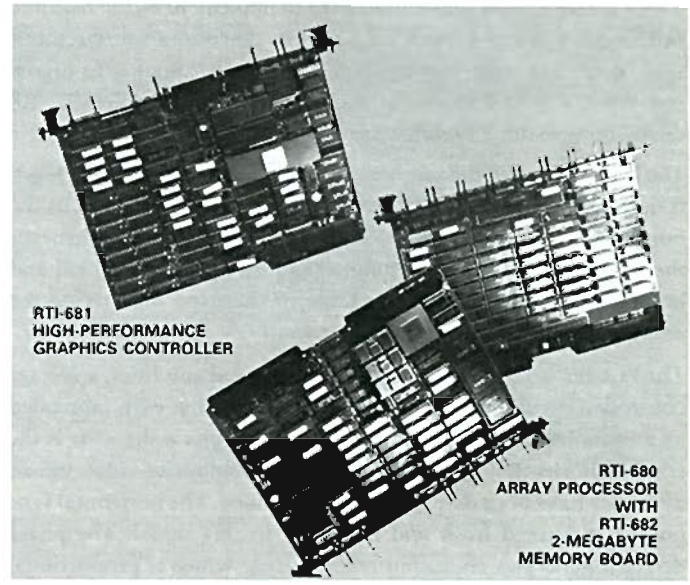
Plug-in boards for standardized buses offer a quick and effective means for a designer to put together a system which provides the basic hardware framework for carrying out an application. These boards are complete functional modules; they will work together because their electrical interfaces and physical form factors meet a carefully defined specification. Basic functions of these plug-in boards include processor, memory, analog and digital input/output, and communications ports.

The VMEbus is one of several such buses that are available today. A relatively powerful bus standard, it supports a 24-bit-wide address bus and a 16-bit-wide data bus; both are expandable to 32 bits under the standard. The physical board size is 233 × 160 millimeters, one of several DIN Eurocard standards.

VMEbus-based systems tend to be used for applications that require more data processing in less time, and more graphics capability without burdening the main CPU of the system. These kinds of applications have created the need for boards such as Analog Devices' RTI-680-HS Array Processor Module and RTI-681-HS Graphics and Video Controller. In addition to making use of the VMEbus standard, they also provide a way to bypass some limitations of the standard bus in applications where performance must not be limited by the bus bandwidth.

THE RTI-680-HS ARRAY-PROCESSOR MODULE

Many applications in signal analysis employ algorithms that require extensive numeric processing at high rates to produce solutions in real time. Digital signal-processing (DSP) microprocessors and microcomputers have architecture optimized for numeric operations, rather than general decision making. The RTI-680-HS uses the Analog Devices ADSP-2100 DSP μP as the computational heart of a high-speed, user-programmable VMEbus board (Figure 1)*. The signal-processing algorithm can be written in either the C language or ADSP-2100 assembly language; the ADSP-2100 operates at 8 million instruction *cycles* per second; since operations can occur in parallel and are completed in one cycle, each cycle can contain multiple instructions.



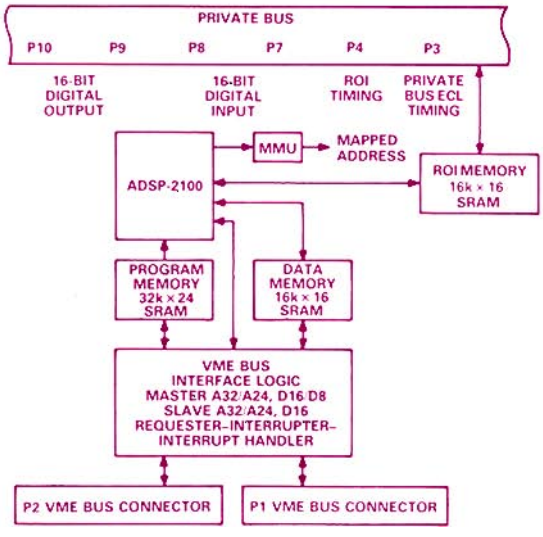


Figure 1. The RTI-680-HS block diagram shows the ADSP-2100 DSP microprocessor, region-of-interest memory, and private high-speed bus.

The RTI-680-HS has features that enhance its performance and bring added capability to many applications. A proprietary private bus, not associated with the standard VMEbus connectors, allows data transfer from on-board memory to other VMEbus boards (equipped with this supplementary high-speed bus) at rates up to 20 megabytes/second, without tying up the VME bus itself. This is especially useful for transferring data to and from the 16K × 16-bit region-of-interest (ROI) memory. The ROI memory is used to store and examine a desired portion of the overall data, such as a digitized video image or sonar signal. The ROI memory is accessed only by the ADSP-2100 and the private bus; it has no impact on the VMEbus memory space or activity.

Both program memory and data memory are provided on board. These memories are separate entities because, unlike the von-Neumann architecture of most standard processors, the DSP microprocessor uses a Harvard architecture with distinct program and data memory areas (including two address buses and two data buses) for more efficient cycle overlapping and pipelining of instruction and data accesses. There are 32K words of 24 bits/word for program, using high speed, zero-wait-state static RAM. The data memory consists of 16K words (16 bits/word), also zero-wait-state static RAM, for maximum throughput. The data memory is dual port, with one port for the ADSP-2100 and the other for the VMEbus. This prevents data-bus contention between local, on-board needs and other VMEbus boards trying to access the memory. A CPU or DMA controller on another VMEbus board can load the memory while the RTI-680-HS is processing data

*Use the reply card for technical data.

which was loaded earlier. This pipelined data transfer eliminates the need to wait for the completion of data load/unload and speeds the execution of many algorithms significantly.

The directly addressable data-memory space of the ADSP-2100 is 16K words of data memory and 16K words of program memory (expandable to 32K), but some applications may need more than this. A memory management unit built into the RTI-680-HS uses a paged table-lookup scheme. Each of 15 mapped pages has a 32-bit mapped-address page register; this allows the physical amount of addressable memory to be increased (using other memory boards) to 4 gigabyte address spaces. The memory mapping scheme uses programmable page (block) offset values to map the logical addresses of the DSP unit into the physical address values.

The entire RTI-680-HS appears to the memory space as a 256K byte block, with a jumper-selectable base address. The board can function as a requester, interrupter, and interrupt-handler module. As a VMEbus master, it operates in D (for *data*)16/D8, A (for *address*)32/A24 modes; as a VMEbus slave, it supports D16, A32/A24 transfers. LEDs on the front edge indicate the board status; Reset, Trap, Halt, Master, and Protected states are shown; in addition there are three user-programmable LEDs. A connector carries timing signals for data transfer of ROI bits on the private bus; there are also 16 digital input and 16 digital output bits for private bus data transfer.

Software development tools are essential to allow a programmer to implement actual applications code. For the RTI-680-HS, the available development environment includes a C compiler, assembler, linker, and interactive debugger. The C compiler supports 16- and 32-bit integer math, 32-bit IEEE floating-point-format math, and in-line ADSP-2100 assembly language. Function libraries, written in assembly language, are included: VME bus block transfers; vector, matrix, and complex math; convolution, correlation, and FFT; statistical functions; and image analysis primitives are callable from the C code.

HIGH-PERFORMANCE VIDEO/GRAPHICS CONTROLLER

High-resolution color-graphics applications with fast updates require specialized circuitry to store the picture-element (pixel) information and retrieve it rapidly, without interfering with overall system operation. To display a monochrome screen of N lines, with M pixels/line, and uniform intensity, requires a memory space of $N \times M$ bits. For more than one color, P bits are needed for each pixel to indicate which one of up to 2^P colors is desired. Any manipulation of the displayed image, such as scrolling, adding predefined graphics elements and icons, and zooming, requires additional memory beyond that directly displayed.

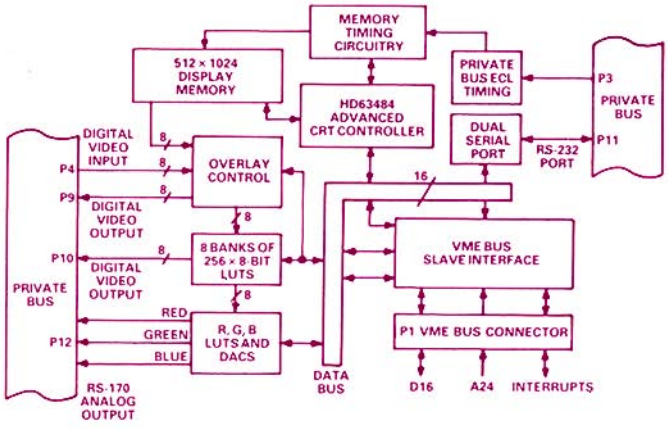


Figure 2. The RTI-681-HS block diagram shows the bus interfaces, dual serial port, and RGB analog output.

The RTI-681-HS* (Figure 2) provides the necessary memory, circuitry, and software-selectable operations to support a color screen with up to 256 colors displayed simultaneously from a total palette of 16.8 million (2^{24}) colors. It provides separate red, green, and blue (RGB) outputs to drive the three color guns of a CRT; monochrome displays can also be connected. The board uses high-level graphics commands which are called by the user's program to implement specific graphics operations. A special design capability allows graphics and live video signals to be overlaid and displayed simultaneously for mixed images. Although compatible with the VMEbus standard, the RTI-681-HS has the same private bus as the RTI-680-HS for achieving high-speed data transfer without tying up the VME intercard bus. The board appears as a 64-byte block of memory in the overall memory space; the address of this block is selected by jumper. These 64 bytes are for the registers which control the board functions, color selection from the overall palette, and operational modes.

The graphics memory capacity is $512 \times 1{,}024 \times 8$ bits (4 megabits), accessed only by the CRT-controller IC at the heart of the circuitry. Of this memory, up to $512 \times 512 \times 8$ bits can be displayed at any time; but the total image may occupy the entire memory. This allows the displayed image to be scrolled up and down; it can also be panned from side to side, and (with some loss of resolution) zoomed in either horizontal or vertical directions (up to a factor of 16×) without having to rearrange the data in memory that represents the image. As an alternative, the memory can be split into two buffers, each $512 \times 512 \times 8$, with one buffer storing the video image and the other storing fonts, icons, and graphic elements that need to be called and displayed quickly, without loading into memory. Any accesses to and from the display memory are available on the next pass of the raster without affecting (i.e., causing glitches in) the currently displayed image.

The task of programming the screen image for graphics is aided by basic commands that can be invoked and then are automatically implemented by the CRT controller IC. There are 38 commands to draw circles, lines, polygons, ellipses, rectangles; fill outlined shapes; copy shapes; etc. Each command consists of its name and a list of parameters which define the subject's size, location, color, and other relevant arguments. A screen image is filled at the rate of up to 2 million pixels per second.

Graphics applications often have related input devices such as a mouse or trackball. The RTI-681-HS has two RS-232 serial points to handle these devices in conjunction with the screen activity. A strobe port is also designed into the board so that a light pen can be used; the strobe signal from the pen causes the screen X and Y addresses to be latched in memory so the location of the light-pen tip relative to the screen image can be determined.

Within a VMEbus system, the board functions as a slave D16, A24 module, capable of transferring data as 16-bit words. In addition to the standard VMEbus connectors, there are connectors for the video output, serial input, private bus, and various other digital inputs and outputs.

TWO NEW MULTIPLE M-DACS SAVE SPACE & POWER IN BOARD DESIGNS

AD396 Quadruple 14-Bit Four-Quadrant Voltage-Output DAC

AD7228 *Octuple* Monolithic 8-Bit Voltage-Output DAC

Multiple digital-to-analog converters in a single package are useful in applications where many DACs are required and cost or space must be saved—or system reliability improved through the reduction of parallel bus wiring. Both of these devices interface to an 8-bit bus, both have voltage outputs (i.e., on-board amplifiers), both retain the flexibility of external fixed or variable references, both take advantage of the low power-dissipation of CMOS, and both are available in versions that meet MIL-STD-883.

THE MONOLITHIC AD7228 OCTUPLE DAC

The AD7228* consists of 8 independent 8-bit DACs with individual amplifiers and latches (Figure 1). Sharing a common 8-bit TTL-compatible input port and a common external analog reference, the DACs are housed in a 0.3-inch-wide 24-pin plastic or Cerdip DIP; they are also packaged in PLCCs and LCCCs.

A three-bit set of address inputs, A0, A1, and A2, determines which latch is loaded when $\overline{WR}$ goes low; the control logic is speed-compatible with most 8-bit microprocessors. The AD7228 will work with either a single 10.8–16.5-volt supply, or (for wider reference range) with an additional V_{SS} supply of −4.5 V to −5.5 V. The required reference for specified performance with a single supply is +10 V; with dual supplies, the range is from +2 V to +10 V.

The AD7228 is available in a choice of six basic performance grades and three temperature ranges (0 to +70°C, −25°C to +85°C, and −55°C to +125°C). With dual supplies, total unadjusted error (K,B,T/L,C,U grades) is ±2/±1 LSB max over temperature; and relative accuracy error is ±1/±½LSB max over temperature; all grades are guaranteed monotonic with differential linearity error ±1 LSB max over temperature. Settling time to ±½ LSB is 5 µs, with a minimum slewing rate of 2 V/µs. Prices begin at $32.00 (100s).

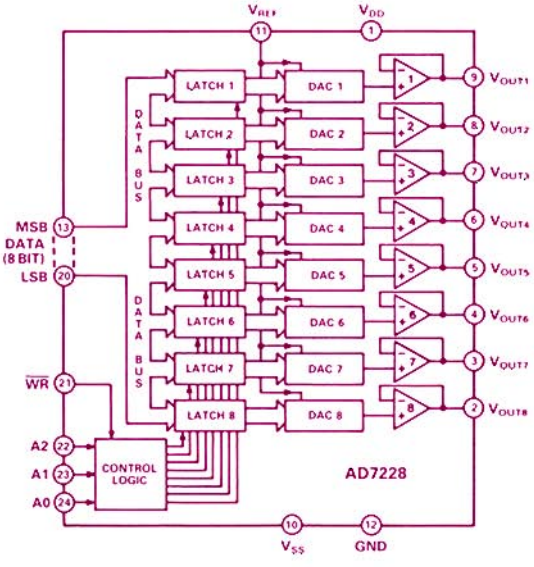


Figure 1. The AD7228 has 8 DACs on a CMOS chip.

*Use the reply card for technical data.

THE AD396 14-BIT QUAD DAC

The AD396* consists of four complete, pre-trimmed (no external trims) 14-bit 4-quadrant CMOS multiplying DACs (monotonic over temperature), with their associated double-buffered registers and amplifiers. The 4-quadrant multiplying DACs accept individually applied fixed or variable analog inputs in the range ±11 V, and multiply them by digitally set gains from −1 to $+(1-2^{-13})$, in steps of 2^{-13}. The device's function can be interpreted as that of either a DAC with bipolar output and a wide range of ± available reference voltages, or a variable-gain amplifier for ac/dc analog input voltages—with 2^{14} values of digitally set positive and negative attenuation.

The DACs (Figure 2) interface to the 8-bit bus via a pair of input data registers and 4 sets of DAC registers, in two bytes—6 (MS) and 8 (LS) bits. A pair of address lines, with the $\overline{CS}$ and $\overline{WR}$ lines, control the device selection and data transfer from the bus, determining whether the LS or MS input register is loaded (or both or neither, or if transparent). A set of four $\overline{CSk}$ lines determine which DAC is loaded (or none or all).

The hybrid AD396 is packaged in a 28-pin hermetic double-DIP available in JD, KD, SD, TD grades. Prices start at $160 (100s).

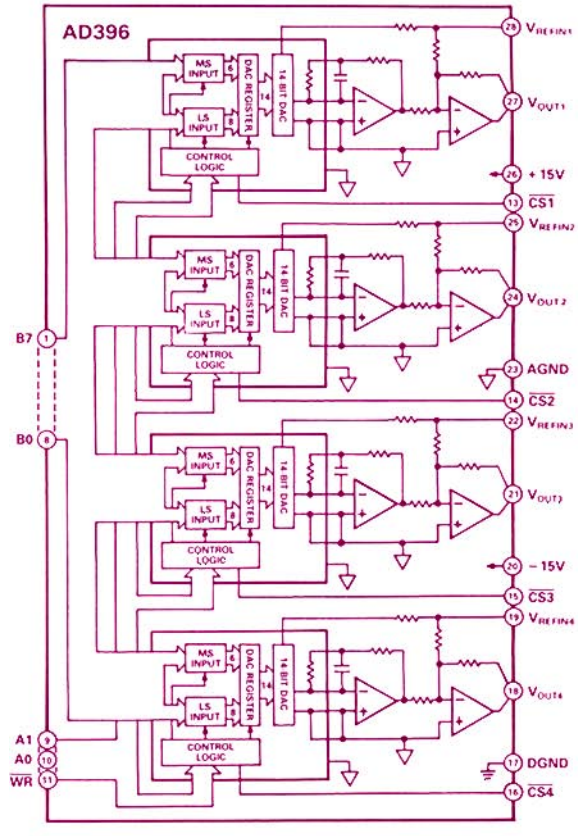


Figure 2. Block diagram of the AD396 quad DAC.

TWO NEW HIGH-PRECISION MONOLITHIC VOLTAGE REFERENCES

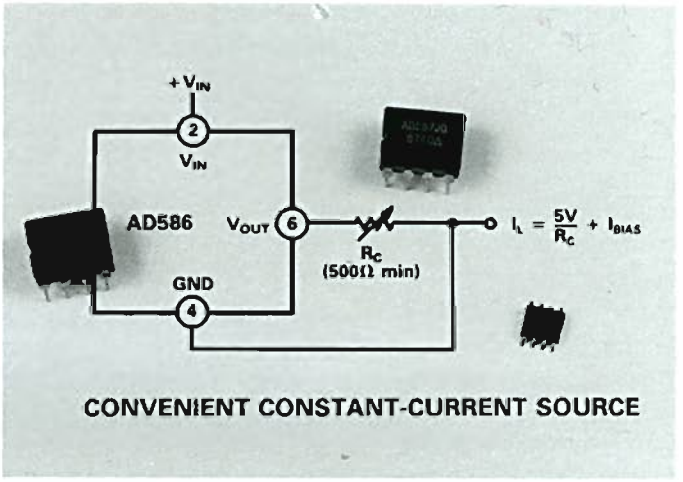
AD586 (+ 5 Volts) & AD587 (+ 10 Volts) Maintain High Accuracy; Buried-Zener Cell, Laser-Trimmed Resistors Reduce Drift and Noise

The AD586* (+5V) and AD587* (+10V) are fixed-output monolithic references characterized by high accuracy, low drift, and low noise. Based on the same proven design as the premium AD588 reference, both devices include a proprietary noise-reduction feature that allows the designer to reduce the already low wideband noise by the addition of a single external capacitor (Figure 1). The buried-Zener-based reference-cell design results in lower noise and drift than can be attained with a bandgap reference. Both devices can be connected as negative-voltage references and as convenient constant-current sources.

Voltage references play an important part in the performance of many circuits and systems. In circuit functions such as DACs, ADCs, and comparators—and in calibration instrumentation, power supply controllers, and data acquisition units, the initial accuracy and long-term drift of the voltage reference set a limit to the performance that can be achieved by the rest of the precision electronic circuitry.

For a voltage reference, the two key specifications are initial offset error and drift. The best grade of the 5-volt AD586 is specified to have an initial error below 2.5 mV, while the 10-volt AD587 has a corresponding error of 5mV; both have a maximum drift of 5ppm/°C (L grade). The long term stability is typically better than 15 ppm/1,000 hours. The reference value can also be "fine-trimmed" with a single external potentiometer to bring it to within "a gnat's eyelash" of the nominal value, or to provide an output voltage that differs from nominal (for example, 5.12 V and 10.24 V are useful values to obtain round-number LSB values in binary applications). The minimum total trim range available is +300 mV, −100 mV.

Both voltage references can source current of at least 10 mA at the specified output voltage. A voltage reference should also have good *load regulation*, that is, stability of the output value with load-current changes. The AD586 and AD587 feature load regulation of 100 μV/mA (J/K/L grades) maximum; this is equivalent to 1 millivolt for a full-scale load change (0.02%, or 1 LSB of 12 bits, for AD586; 0.01%, or 1 LSB of 13 bits, for AD587). Line regulation—output variation with changes in power supply voltage—is 100 μV/V maximum. The +5-volt AD586 will handle a power supply range of 10.8 to 36 V; the +10-volt AD587 requires +13.5 to +36 V. Quiescent currents are less than 5mA.



Output Noise In precision systems, noise is a limiting factor on the final resolution of the circuitry. The peak-to-peak noise output of these references is typically less than 4 μV in the 0.1-to-10 Hz band, and below 200 μV for bandwidths up to 1 MHz. The 100-nV$\sqrt{Hz}$ wideband noise of the buried-Zener cell is less than that of the traditional bandgap reference but still greater than that of the op amp. For lower-noise applications, an external capacitor can be added between pin 8 and ground; with the 4-kΩ R_S and the Zener resistances, this forms an internal low-pass filter. When C_N = 1 μF, the noise is reduced to about 160 μV p-p (Figure 2), with a −3-dB frequency of 12 Hz.

The five performance grades of the AD586 and AD587 are available in 8-pin Cerdip packages and specified for two temperature ranges, 0 to +70°C and −55°C to +125°C; both devices are also available in chip form for hybrid-circuit designs. Six grades are available, including three MIL-temp-range versions. Pricing starts at $2.95 (JQ grade in 100s). Small-outline IC packaging will be available in the future.

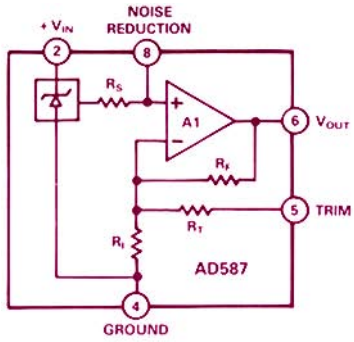


Figure 1. Functional block diagram of the AD587. The AD586 is similar but uses a voltage divider on the Zener output.

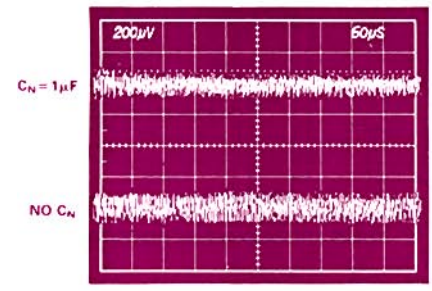


Figure 2. Effect of 1-μF noise-reduction capacitor on broadband noise.

*Use the reply card for technical data.

MONOLITHIC ELECTROMETER HAS 60 fA *max* BIAS CURRENT

AD549 Also Has Low Offset, Drift, and Settling Time

Top-Gate FETs in Standard Process Technology for Low Cost

by JoAnn Close

The AD549* is a high-performance monolithic electrometer operational amplifier. Besides having ultralow bias current, it is laser-trimmed for low offset voltage and drift. The AD549 is exceptionally useful for sub-picoampere current-measurement or interfacing with impedances greater than $10^8\Omega$. It can be used to great advantage in the design of photodiode preamps, pH electrode buffers, electrometers, and vacuum ion gauge measurements—as well as in precision integrators and low-droop track-holds.

The AD549's ultralow input current is achieved with "Topgate" JFET technology, a process development exclusive to Analog Devices.[1,2] This technology allows fabrication of extremely low-input-current JFETs—with electrically isolated front and back gates—compatible with a standard junction-isolated bipolar process. The bootstrapped input stage, one of the techniques used in the AD549 to minimize bias current, insures that the input current is essentially independent of common-mode voltage. Common-mode input impedance typically exceeds $10^{15}\Omega$.

In addition to its low bias current, offset, drift, and noise (Figure 1), the AD549 has a small-signal bandwidth of 1 MHz, slew rate of 2 V/μs, and settling time of 4.5 μs to 0.01% of final value for a full-scale output step. The AD549 conserves power, with maximum (tested) quiescent supply current of 700 μA; this also minimizes heating effects on input current and offset voltage.

The AD549 is available in a choice of grades optimized for specific applications. The AD549L provides the best current resolution with a maximum warmed-up bias current of 60 fA (i.e., 60×10^{-15}A) at either input and any voltage in the ± 10-volt common-mode range at 25°C; its offset and drift are 0.5 mV and 10 μV/°C (0° to 70°C), max. The AD549K, for the best combination of bias current and voltage offset, has 100-fA max bias current, 0.25 mV offset, 5 μV/°C drift, and guaranteed max 0.1-10 Hz noise of 6 μV p-p.

There are also a lower-priced AD549J—where cost-performance tradeoffs are permissible—and a MIL-temp-range AD549S (with 883 version available). Extended-reliability PLUS screening is also

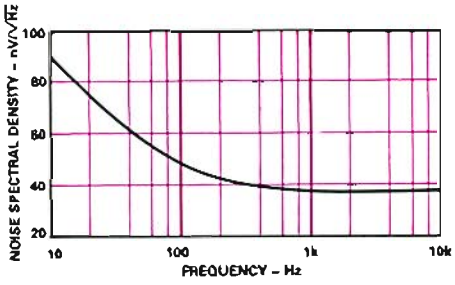
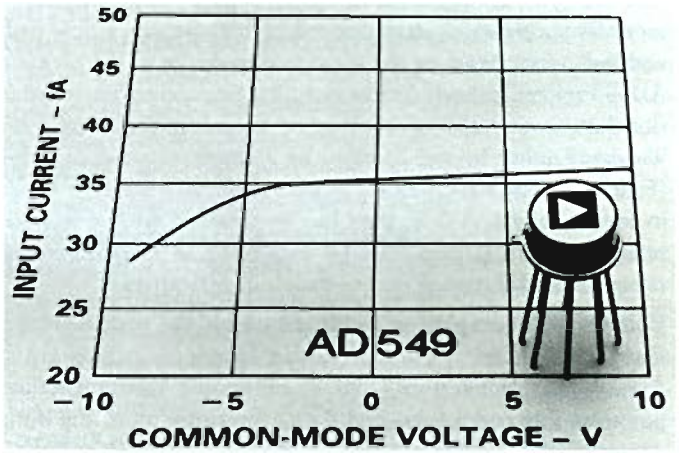


Figure 1. Input voltage-noise spectral density.



available for commercial-temperature-range devices. Prices in 100s for AD549JH/KH/LH/SH are $8.95/$12.50/$15.45/$32.50.

The AD549 is packaged in a hermetic TO-99 metal case, connected to pin 8, which can be driven as a guard at the same potential as the inputs. This minimizes exposure of the input terminals to noise and leakage current. The AD549's pinout is compatible with earlier hybrid electrometer amplifiers, including the AD515, OPA104, and 3528, offering instant performance improvement.

To fully exploit the AD549's low input current requires careful design and execution of the external circuitry. High-impedance input leads ideally should be short, shielded, and connected to standoffs made of high-resistivity material (e.g., Teflon).

Figure 2 shows package connections and hookup for a follower-with-gain. The case and external guards are driven from the low-impedance feedback point (for long leads or noisy environment, buffer the driven items from the feedback point by a follower).

Because of its extremely low leakage, the AD549 can be used in testing low-level leakage characteristics of electrometer circuits, measuring photodiode outputs at low light levels, and as a log-ratio amplifier for comparing wide-dynamic-range signals, when used with an appropriate dual log-transistor. It can also be used with high-impedance electrodes to measure ion concentrations.

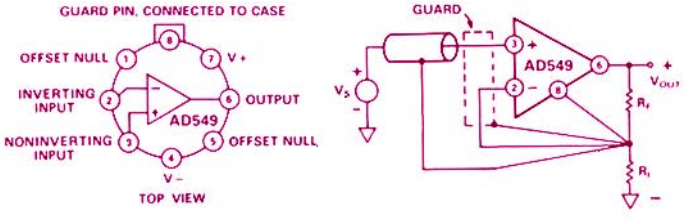


Figure 2. Guard pin for reduced leakage and current noise. a. Connection diagram, showing guard pin. b. Non-inverting amplifier with guard.

*Use the reply card for technical data.

[1]Close, JoAnn P., and Lewis Counts, "A 50-fA Input Current Junction-Isolated JFET Op Amp," *Digest of Technical Papers*, 1986 IEEE International Solid-State Circuits Conference.
[2]U.S. Patent 4,639,683.

HIGH-PERFORMANCE ANALOG INPUT BOARDS FOR IBM PC-AT

High-Accuracy RTI-850 Features 16-Bit Resolution

High-Speed RTI-860: 12-Bit/250-kHz—Or 8-Bit/330-kHz—Throughput

The RTI-850* (Figure 1) and RTI-860* (Figure 2) are complete, high-performance analog input boards for operation with the IBM PC-AT. They interface to the computer in similar ways, but the RTI-850 emphasizes 16-bit resolution and 14-bit (to 0.003% of full scale) accuracy, while the the RTI-860 has high throughput—250 kHz for 12-bit resolution, with up to 16 single-ended channels.

Both boards can operate without the supervision of the PC-AT's CPU. The boards can be triggered from external TTL pulses, analog input-voltage values, auxiliary analog voltages, or software. The hardware-based analog triggering circuitry allows paced groups of a/d conversions to be initiated by real-world signal-level crossings. This trigger function is unique and up to 1,000 times faster than with conventional IBM-compatible I/O boards that have software triggering only. Also available are buffer memory for up to 256K samples, on-board pacing functions, and the capability of multiple-board synchronization.

A pre-trigger mode of data acquisition allows the user to take data prior to, during, and after receiving the trigger. This improves response time by avoiding software delays; it also prevents loss of data samples while the board is responding to the trigger input.

On-board RAM allows data to be acquired and stored in the card's local memory without using the PC-AT's CPU. On the other hand, DMA transfer into AT system memory allows incoming data to bypass the card's memory completely.

RTI-850. The RTI-850 has a throughput of 50 kHz at 16-bit resolution; a 10% increase can be gained by short-cycling to 14 bits. Typical applications for the RTI-850 include analytical and medical instrumentation, robotics and precision machine control, and test equipment. The RTI-850 list price is $2,095.

RTI-860. The RTI-860's throughput can be increased to up to 330 kHz by short-cycling to 8 bits. The RTI-860 is useful for such

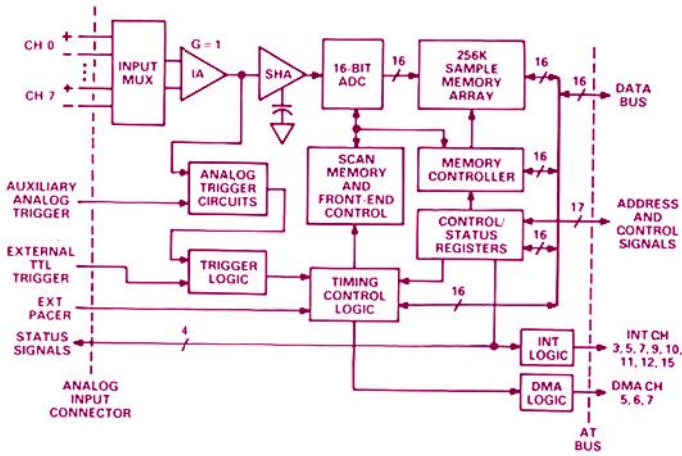
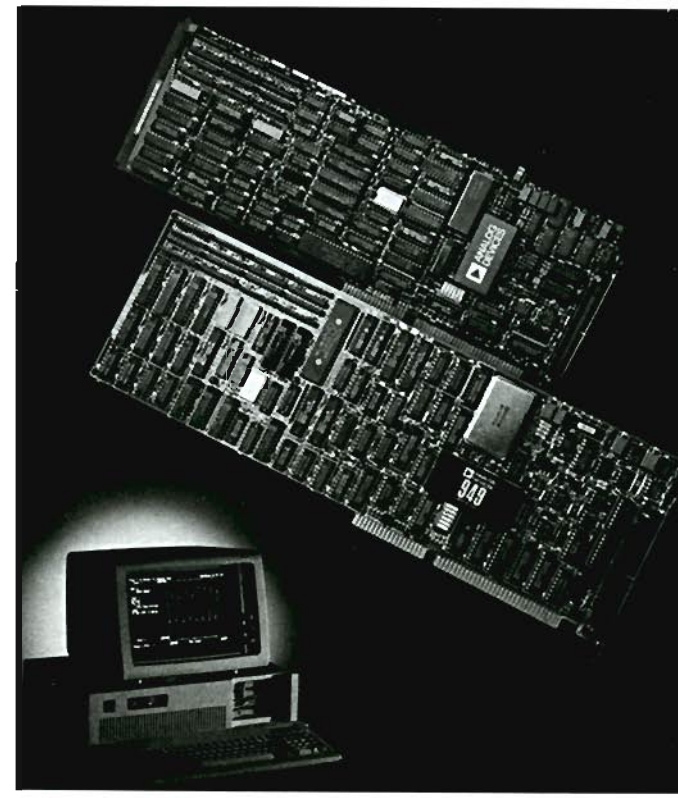


Figure 1. Block diagram of RTI-850 shows 8-channel differential input multiplexer and 16-bit ADC.

* Use the reply card for technical data.



applications as spectral, correlation, and vibration analysis, machine monitoring, and test equipment. It lists for $2,395.

Optional accessories include software support (AC1527-B) for use by both programmers (drivers) and non-programmers (menu-driven software). A screw-termination panel (STB-GP) makes available both direct connection to signal sources and remote signal conditioning.

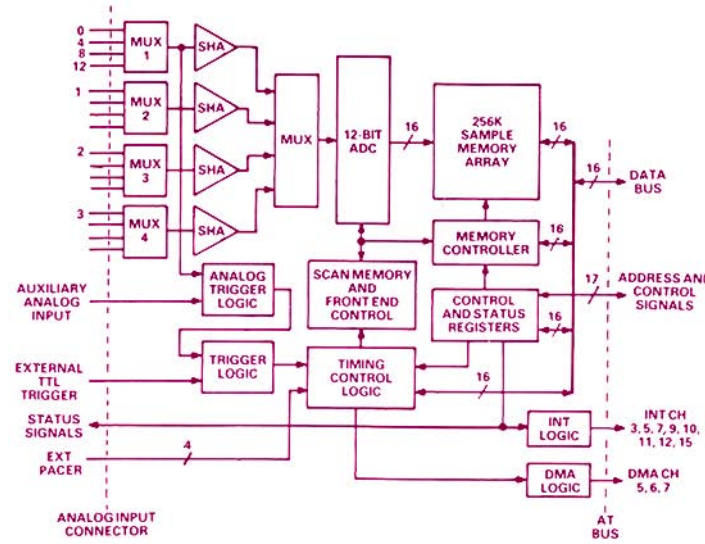


Figure 2. RTI-860 has 4 track-holds to ensure that data is immediately ready for the next conversion.

FAST-SETTLING 12-BIT DAC PROVIDES 40-ns µP INTERFACING

AD767 Is Functionally Complete In 0.3" Skinny DIP Package Includes Latches, D/A Ladder, Reference, Output Amplifier

The Analog Devices AD667* was introduced in 1984 (Analog Dialogue Vol. 18, No. 2) to provide circuit designers with a low-cost, functionally complete 12-bit DAC. Since that time, the clock speeds of microprocessor-based systems have increased considerably, along with circuit densities. A new 12-bit monolithic bipolar DAC, the AD767* (Figure 1), provides a complete analog voltage-output function—with a *write* strobe requirement of only 40 ns—in a narrow (0.3-inch wide) DIP. The output has a maximum linearity error of ± ½ LSB and guaranteed monotonicity over the entire operating temperature range. Precision high-speed current steering switches and a laser-trimmed thin-film resistor network are key to its high-speed, high-accuracy performance.

The short strobe time allows the AD767 to interface directly to the fastest microprocessor busses (such as the 68000, 8086, TMS32010/20/C25, and ADSP-2100 families), eliminating the need for processor *wait* states or pulse-stretching circuitry. The digital interface accepts data from the bus as a single 12-bit parallel word, with CMOS- and TTL-compatible input levels. The input gates draw less than 10 µA, to minimize loading on the bus drivers; a single low-power Schottky gate can drive several AD767s on a common bus. Figure 2 shows how the AD767 is interfaced to the ADSP-2100 DSP microprocessor; the data sheet* shows equally simple interfacing to other popular DSP processors.

The analog output settles to ½ LSB in under 3 µs for a 10-volt full-scale transition. An internal buried-Zener reference (for high stability) is trimmed to 10.0 ± 0.1V. This reference voltage is used for the DAC switches; it is also available for external applications and can supply up to 1 mA of current to external loads. On the other hand, an external reference can be used, with the internal reference ignored. The recommended range for an external reference is from +8 to +10.5 V; this includes the popular full-scale ranges of 8.192 V and 10.24 V.

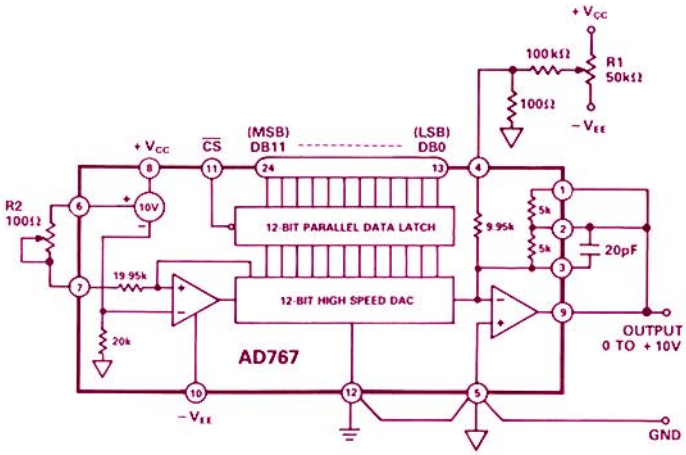
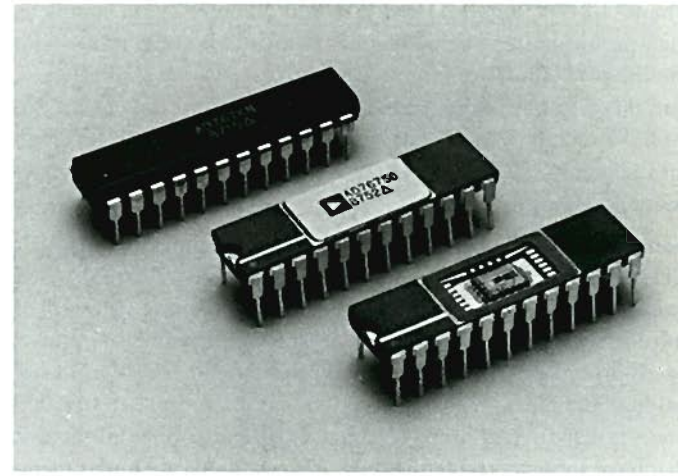


Figure 1. Functional block diagram of the AD767 configured for 0 to +10V unipolar voltage output.

*Use the reply card for technical data.



ANALOG OUTPUT CONNECTIONS

The versatility of the AD767 is enhanced by the wide selection of output ranges that are available by pin-strapping. Internal scaling resistors provide bipolar output ranges of ±10, ±5, and ±2.5 V and unipolar output ranges of 0 to +5 V or 0 to +10 V. The internal resistors save cost compared to external resistors; more important, they perform far better with far less drift error. The thermal variations of the internal scaling resistors track one another closely, minimizing drift of offset and gain—the typical full-scale-gain temperature coefficient is only 5 ppm/°C. *External* feedback resistors for the output amplifier generally produce excessive gain-drift errors in most applications.

In some situations, the maximum output amplifier current—5mA—is not sufficient, or the DAC output must be combined with some other signal. The summing node of the AD767 output amplifier is accessible for current boosting and gain ranging, or for tailoring dynamic response.

The device will operate with standard ±12-volt or ±15-volt dual power supplies; power consumption is typically 400 mW. Prices start at $8.40 (1,000s) for plastic DIPs specified for 0 to 70°C operation; ceramic packages are also available with wider temperature range specifications.

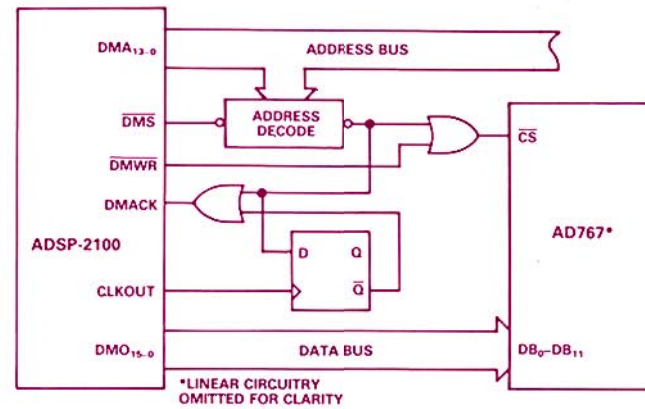


Figure 2. Interfacing AD767 to ADSP-2100 microprocessor.

HIGH-RESOLUTION MONOLITHIC RESOLVER-TO-DIGITAL CONVERTER

2S80 Has Choice of 10-, 12-, 14-, and 16-Bit Resolutions
Velocity Output Available; Temp Ranges Include −55°C to +125°C

by John Malcolm

The Analog Devices 2S80* is a monolithic resolver-to-digital converter on a single monolithic chip, housed in a 40-pin ceramic DIP. The industry's highest-resolution (and the only tracking) monolithic RDC, it is pin-programmable for 10-, 12-, 14-, and 16-bit resolution. At 10-bit resolution, it can track resolvers at up to 1,040 revolutions per second, and at 16 bits, it can still track at nearly 1,000 rpm. It has a velocity output linear to ±1%, eliminating the need for a tachometer in servo-control applications.

The 2S80 is a trimmed version of the 2S81 RDC chip, introduced in the last issue (*Analog Dialogue* 21-1, "First Monolithic Resolver-to-Digital Converter"). Manufactured in a proprietary bipolar/CMOS process (BiMOS), the chip combines high speed, high-accuracy bipolar circuitry, and dense, low-power CMOS logic (power dissipation is typically 300 mW).

Three accuracy grades are available for each of two operating temperature ranges—2S80JD/KD/LD for 0°C to +70°C and 2S80SD/TD/UD for −55°C to +125°C (MIL-STD-883 qualification is in process). The LD/UD grades are accurate to within ±2 arc-minutes, followed by the KD/TD (±4 arc-minutes) and JD/SD (±8 arc-minutes). Repeatability is to within ±1 LSB for all grades. The device operates from a ±12-volt power supply—and a +5-V logic supply. Prices (100s) start at $89.10 for the 2S80JD.

Figure 1 shows the basic elements of resolver/digital angular measurement. The resolver is a rotating transformer with a rotor winding and a pair of stator windings that are physically 90° apart. Modern resolvers avoid slip-ring connections by an additional pair of windings for excitation of the rotor. An ac reference source (50–20,000 Hz, for the 2S80, depending on system requirements) is applied to the rotor. The stator outputs represent the sine and cosine components of a unit vector whose angle is equal to the angular position of the rotor with respect to the stator.

A 2nd-order tracking loop is used to convert to digital (Figure 2); a feedback system continually updates the conversion result. The ratio multiplier compares the angle between the resolver inputs

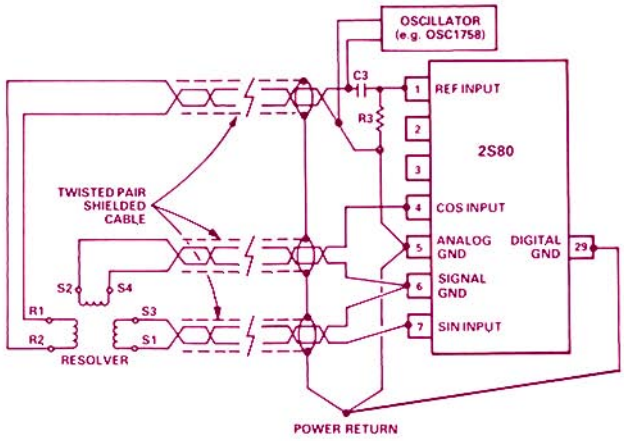
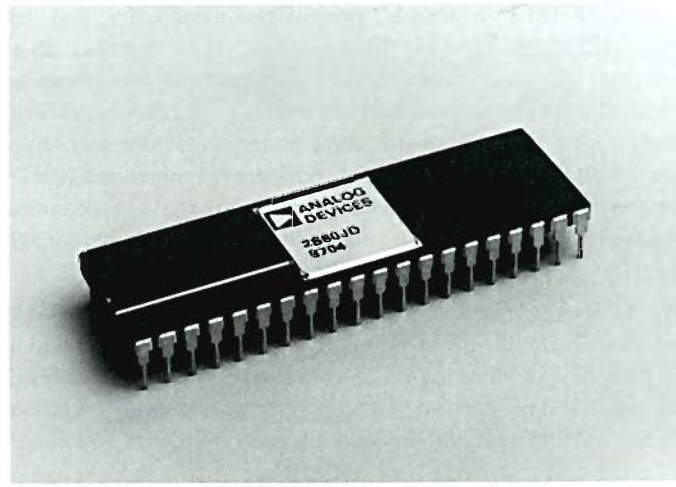


Figure 1. Resolver and resolver-to-digital converter.

*Use the reply card for technical data.



with the digital angle stored in its counter. The result is an ac error signal proportional to the sine of their difference; it is compared with the ac reference in a phase-sensitive demodulator, and the resulting dc error signal is integrated—to get rid of noise and amplify the low-frequency error. The integrator output drives a voltage-controlled oscillator (VCO), which produces a train of pulses at proportional frequencies with polarity ("direction") identification.

The pulses are applied to a counter; its output is the digital angle to be compared with the measured angle. The error signal produces a count in the appropriate direction to increase or decrease the angle to minimize error. When steady-state *angle* output is reached, the average count is not being incremented, i.e., the average VCO input is zero; but for zero integrator output, there is no accumulation of average error, so the average error is also zero. For steady-state *speed*, the counter pulses arrive at a constant rate, which means constant VCO input and zero integrator input (i.e., *zero average error*); note that the integrator output (VCO input) is thus a measure of speed.

Since no two applications have similar dynamic performance requirements, the bandwidth, maximum tracking rate, and velocity scaling of the 2S80 are set by the user, using externally connected low-cost preferred-value resistors and capacitors. Data is transferred via a 2-byte, 16-bit output data latch to either an 8- or a 16-bit bus. All logic levels are TTL-compatible. The latest value of the angle count is always available within 1 clock cycle.

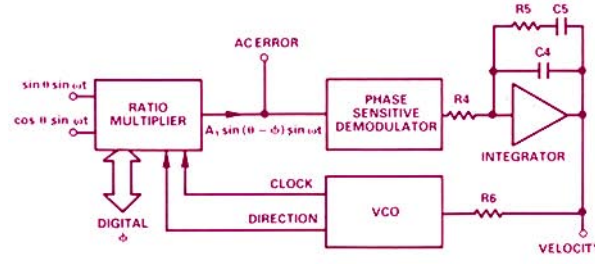


Figure 2. Functional diagram of the 2S80.

64-BIT FLOATING-POINT CHIP SET WITH 40-MFLOPS THROUGHPUT

ADSP-3212 Multiplier & ADSP-3222 ALU Have Single Pipeline Stage
Conform to IEEE-754 Format; DEC-Format Options Also Available

The ADSP-3212* is a 64-bit floating-point multiplier, and the ADSP-3222* is a 64-bit floating-point ALU; together they comprise the basic computational elements for implementing a high-speed numeric processor. As a chip set, they are capable of 40-MFLOPS throughput for single-precision, double-precision, and 32-bit fixed-point operations. Both are manufactured in a 1-micron (*drawn*) double-metal CMOS process; each chip consumes less than 1 W. They are a pin-compatible performance upgrade for the ADSP-3211/3221 Floating-Point Chipset (*Dialogue* 21-1).

The ADSP-3212 incorporates an internal 54 × 54 array multiplier; this permits double-precision multiplications to be executed in a single cycle. In addition, it has on-chip circuitry to handle fast IEEE division: 300 ns maximum throughput for a single-precision *divide*, and 600 ns maximum for double precision.

Both the ADSP-3212 and the ADSP-3222 have a single internal pipeline register (Figure 1). Unlike multipliers that deliver fast throughput by using multiple pipeline stages, these devices have less chip latency (time required from *data in* to *data out*) and easier software development. The ADSP-3212 and ADSP-3222 require only 130 ns maximum from the time 32-bit data is read in to its availability at the output pins, an important capability in scalar processing and in executing algorithms with sequences of operations that depend on the data. Packaged in a 144-pin grid array, there are two grades: "J", for 16.7 MFLOPS per device, and "K", for 20 MFLOPS per device. Prices (100s) start at $297.

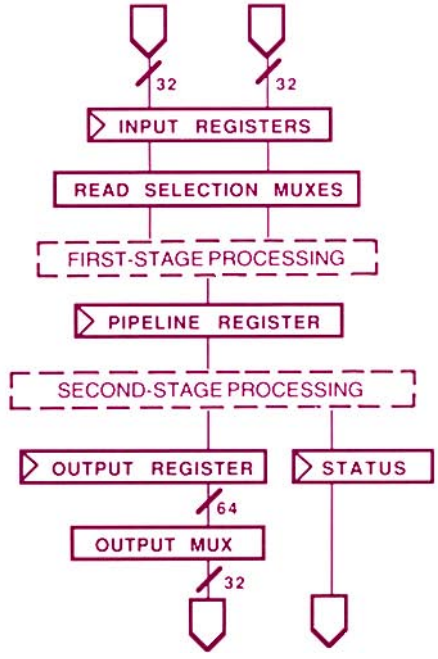
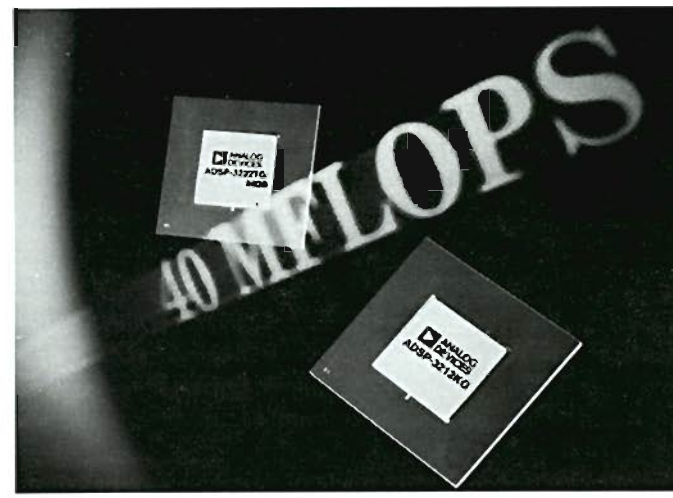


Figure 1. Generic architecture of ADSP-32XX number-crunchers.

*Use the reply card for technical data.



Both devices support 32-bit and 64-bit IEEE-754 floating-point operation, as well as 32-bit fixed-point twos-complement, unsigned magnitude, and mixed-mode arithmetic. Versions that support DEC formats F and G (the ADSP-3213 and ADSP-3223) are also available. Typical applications include high-performance digital signal-processing, engineering workstations, floating-point accelerators, array processors, mini-supercomputers, and RISC (reduced instruction-set computer) processors.

In conforming to IEEE Standard 754, these chips ensure complete software portability for computational algorithms adhering to the Standard. All four rounding modes are supported for all floating-point data formats and conversions. Five IEEE exception conditions—overflow, underflow, invalid operation, inexact result, and division-by-zero—are available as state flags. The IEEE gradual underflow provisions are also supported, with special instructions for handling denormals. An alternative FAST mode sets numbers less than the smallest IEEE normalized values to zero, eliminating exception handling when less than full conformance to the Standard is permissible.

Both chips have internal feedback paths from the output to four of the eight input registers—and feedforward paths from all input registers to the output register. Feedback to both banks of input registers makes it easier to interleave partial sums and partial products for maximum throughput. The internal feedback paths eliminate the need to use an external 64-bit bus to transfer data between the device's output and input registers—with the associated time penalty.

The instruction set is oriented to system-level implementations of function calculations. Specific instructions facilitate such operations as table lookup, quadrant normalization for trigonometric functions, extended-precision integer operations, logical operations, and conversions betweeen all data formats. Exact floating-point division and square root are supported directly.

HIGH-SPEED SINGLE & DUAL MONOLITHIC LATCHING COMPARATORS

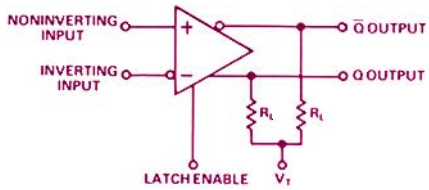
AD96685/87 Have 3.5-ns max Propagation Delay, 50-ps Dispersion Low Power Dissipation, ECL-Compatible Outputs, Choice of Packages

The AD96685 and AD96687* are high-performance monolithic single- and double comparators (Figure 1). With propagation delay of 3.5 ns, max (2.5 ns typical), and propagation-delay dispersion of 50 picoseconds, they are comparable in speed to the AD9685 and AD9687, faster than many other 685/687 devices, and lowest in specified propagation-dispersion among devices in this class. They are also among the lowest in dissipation (135 and 270 mW).

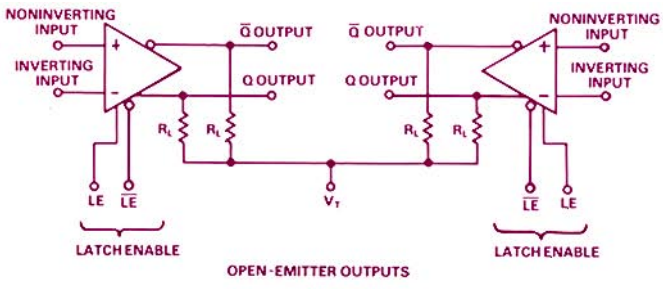
Propagation delay, the time to make a decision, is defined as the time required for an input pulse of 100 mV, overdriving the threshold by 10 mV, to swing the output to the 50% transition point. *Delay dispersion*, a measure of the dependence of propagation delay on input swing, is defined as the change in propagation delay from 100-millivolt to 1-volt overdrive.

Besides speed of response, accuracy is important. With an input range of −2.5 volts to +5 volts, these devices have high-precision differential input stages with maximum offset of 2 millivolts at +25°C and 3 millivolts over the temperature range. Minimum common-mode rejection is 80 dB; and the maximum drift rate is 20 μV/°C. Maximum bias current is 10 μA (13 μA over temperature) and max offset current is 1.0 μA (1.2 μA over temperature).

They perform decisions based on threshold-crossing—by analog (or digital) voltages—rapidly and accurately in all kinds of applications; for example, in automatic test equipment, they would be used in pin-receiver electronics and delay generators; in bench instrumentation, they are useful in triggering; in nuclear instrumentation, for high-speed-event detectors. Since comparators are essentially fast , accurate, one-bit a/d converters, they can be used to make decisions in a variety of conversion applications,



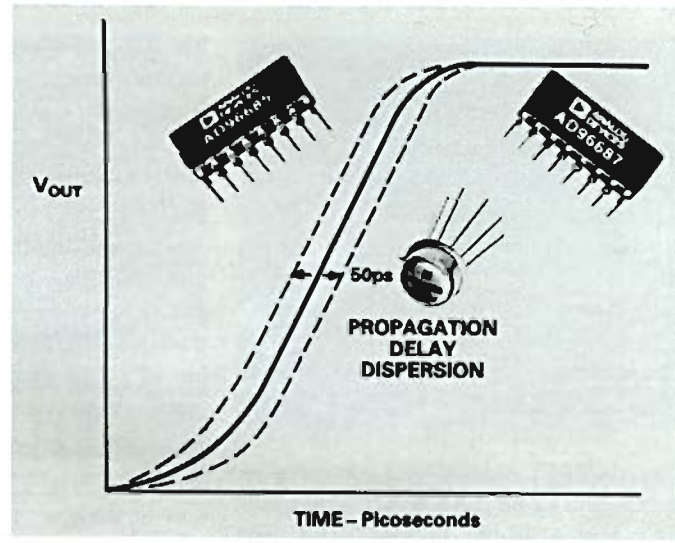
a. AD96685.



b. AD96687.

Figure 1. Functional block diagrams.

*Use the reply card for technical data.



especially those involving unusual architectures where an off-the-shelf ADC with appropriate characteristics isn't available.

Figure 2 shows the elements of an application as a window comparator. The output is *high* when V_{IN} is greater than $+V_{REF}$ or less than $-V_{REF}$, and *low* for values in between.

The digital outputs are ECL-compatible, with 30-mA output capability for driving 50-ohm-terminated transmission lines. A latch-enable allows the devices to operate in the sample or track mode. In *sample*, the output remains latched in the previous state until given a short enable pulse which allows a new decision to be made, then latches it. In the *track* mode, the output takes on whatever sequence of states is dictated by the varying inputs until the latch signal freezes the most-recent decision.

The devices require +5-volt and −5.2-volt supplies and are specified for operation over temperatures from −25°C to +85°C (BH, BQ) or −55°C to +125°C (TE, TH, TQ). Both devices are available in either a 16-pin ceramic DIP or a 20-terminal LCC. The AD96685 single comparator is also offered in a 10-pin TO-100 metal can. Prices for the AD96685/AD96687 (100s) start at $4.60/$6.40.

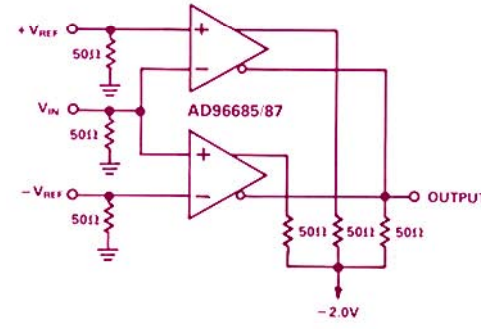
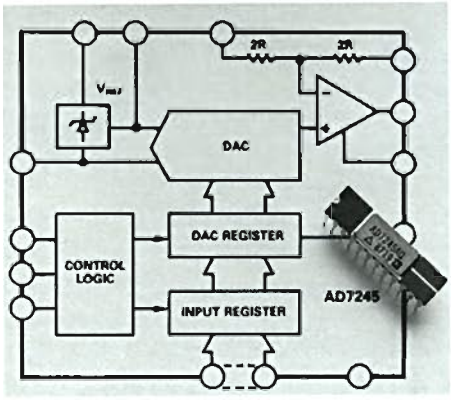


Figure 2. Basic connections for high-speed window comparator.

COMPLETE 12-BIT CMOS DACS

With Reference, Output Amp
AD7245/48 for Choice of Bus



The AD7245* and AD7248 are complete monolithic 12-bit CMOS d/a converters, housed in a 24-pin "skinny" DIP. The LC²MOS (linear-compatible CMOS) process makes it possible to include the DAC, output amplifier, voltage reference, control logic and double-buffer latches on a single compact chip.

The AD7245 accepts data in a 12-bit broadside format; the AD7248 provides an 8 + 4-bit interface for 8-bit buses. Both devices are double-buffered; this makes simultaneous update possible in multi-DAC systems without added logic circuitry.

While featuring fast (5-µs) settling time, the DACs have 135-mW maximum dissipation. Both operate on a single or dual 15-V supply. For application flexibility, user-selectable pin-strap ranges are 0 to +5 V and 0 to +10V (with single supply) and ±5 V with dual supplies.

Both models have high-speed logic (80 ns) for direct interface to most microprocessors. An asynchronous "clear" ($\overline{CLR}$) signal on the AD7245 simplifies resetting to a known condition after powerup or system fault.

Laser wafer-trimmed thin-film resistors eliminate gain and offset trims, saving space. Three different packages are available, including a 24-pin 0.3" DIP, an LCC and a PLCC. Monotonicity is guaranteed for three temperature ranges: the J grade (0°C to +70°C), A grade (−25° to +85°C), and S grade (−55° to +125°C). Prices for both models start at $9.85 (J grade). ▶

*Use the reply card for technical data.

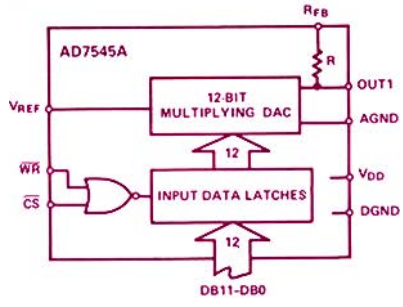
IMPROVED PIN-COMPATIBLE UPGRADE FOR AD7545 SOCKETS

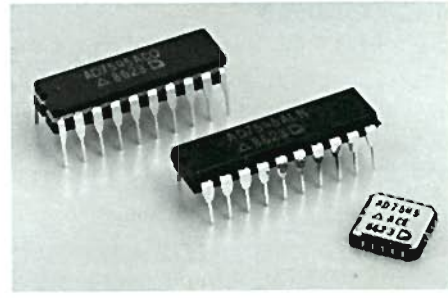
The AD7545A M-DAC: Faster, More Accurate, Lower in Cost
All Grades are 12-Bit Accurate, Have 100-ns Bus-Access Time

The AD7545A* is a 12-bit CMOS multiplying d/a converter with internal data latches. It is an improved pin-compatible update of the AD7545, which we originally introduced in 1982 (Dialogue 16-1, p. 19) and has since become an industry standard.

Among the improvements is a threefold reduction in bus-access timing—from 280 ns to 100 ns—permitting this industry-standard DAC to connect directly to fast 16-bit µP's and eliminating inefficient *wait* states in hardware or software.

Also, unlike its predecessor, the AD7545A





has ±1-LSB maximum gain error when powered from a single +5-volt supply; this provides high precision in 5-volt operation (with both TTL and CMOS compatibility).

Drawing a maximum supply current of 2 mA, the AD7545A is specified for operation with a +15-volt supply as well as with +5 V. Six grades are rated over three temperature ranges: 0 to +70°C, −25°C to +85°C, and −55°C to +125°C. Packages include a 20-pin plastic or ceramic DIP and a 20-terminal PLCC or LCCC. Prices in 100s start at $7.55. ▶

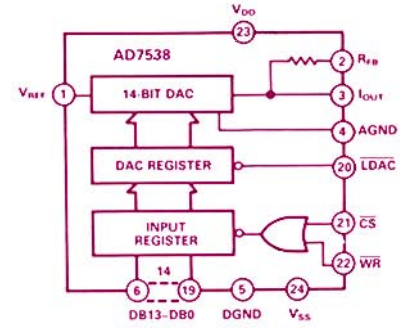
14-BIT-RESOLUTION-AND-ACCURACY MONOLITHIC CMOS M-DAC

All Grades of AD7538 Are 14-Bit Monotonic Over Temperature
Lowest-Priced Version, Untrimmed, Beats Premium 12-Bit DACs

The AD7538* is a CMOS multiplying d/a converter that provides 14-bit resolution and accuracy over its full specified operating temperature range. The lowest grade has high accuracy and stability for 12-bit applications without needing external trims—at prices competitive with 12-bit DACs. (The AD7538JN is $10.50 in 100s.)

Microprocessor compatibility and double-buffered data latches allow simultaneous update in systems using multiple DACs. Applications for the AD7538 include digital audio, µP-based control systems, precision servo control, and measurement and control in wide-temperature-range environments.

Maximum differential nonlinearity is ±1 LSB for all grades over temperature, and maximum relative-accuracy error is ±1 LSB max (K/B/T over temperature). Packaging in a 24-pin 0.3" DIP ensures that



designers do not have to pay a space or cost penalty for its resolution & accuracy.

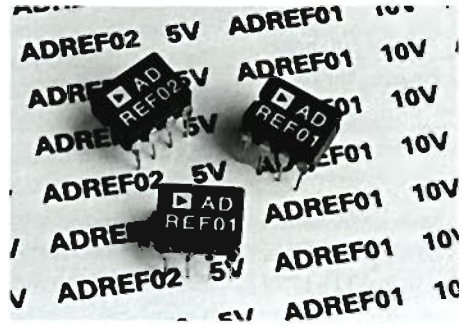
A current-output DAC, it is parallel-loaded by a single 14-bit word, using standard chip-select and memory-write commands. Operating from +12 to +15-volt supplies, it draws low power, 60 mW maximum. Its output-current settling time is 1.5 µs, maximum. Both TTL and CMOS logic inputs are accepted. ▶

TWO NEW REFERENCES WITH EXISTING 2ND SOURCES

10-V ADREF01 and 5-V ADREF02 Have Lowest Noise Hermetic Cerdip-Packaged Devices at Plastic Prices

The ADREF01* and ADREF02* are low-noise, high-performance 10- and 5-volt references for all applications where the higher grades of industry-standard REF01 and REF02 are specified. All Analog Devices grades are housed in an 8-pin cerdip package, for hermeticity and machine-insertability at a price comparable to that for non-hermetic plastic.

The ADREF01 has a laser-trimmed output of 10.00 volts ±30 mV max (AQ and EQ grades) and ±50 mV max (HQ and Q); max temperature drift is ±8.5 and ±25 ppm/°C, respectively. Typical output noise is 4 μV p-p, 0.1 to 10 Hz, and long-term stability is 15 ppm per 1,000 hours. Grades EQ & HQ perform as specified from 0 to +70°C, and AQ and Q operate from −55 to +125°C, with /883 versions available. Prices start at $2.95 (ADREF01HQ, in 100s).



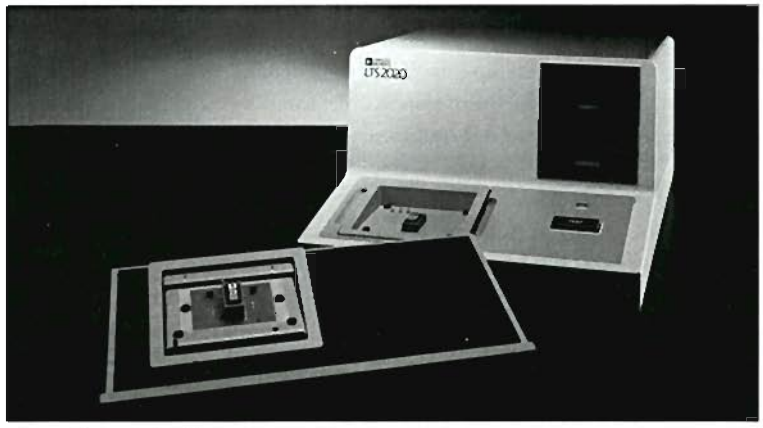
The ADREF02's output is trimmed for 5.00 volts ±15 mV max (EQ and AQ) and ±25 mV max (HQ and Q), with maximum temperature drift of ±8.5 and ±25 ppm/°C, respectively. Noise and long-term stability are similar to those of the ADREF01, as are the operating temperatures for the various grades. Prices are like those of ADREF01. They start at $2.95 (HQ in 100s).

SWITCHES TESTED ACCURATELY ON BENCHTOP TESTERS

Add Switch-Test Capability to LTS-2000 Series LTS-2700 Family Board Tests Switches and Multiplexers

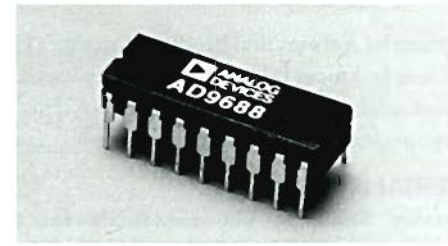
The LTS-2700 Switch Family Board,* used with the Analog Devices LTS-2000 series of benchtop testers, can test dc parameters of both switches and muxes—including leakage (with accuracy to within 50 pA). This capability adds to the LTS-2000 series' ability to test linear, digital, data-conversion, and discrete devices.

With the *Create* software, the board facilitates data logging of test results at Incoming Inspection and in semiconductor manufacturing. It includes the software power for use in component-evaluation applications. It tests *off* leakage, *on* leakage, source-to-drain *on* resistance and Δ*on*-resistance, digital input currents, and supply currents.



FAST 4-BIT FLASH ADC

AD9688:200 Msps Encode Rate 7-Bit Differential Linearity

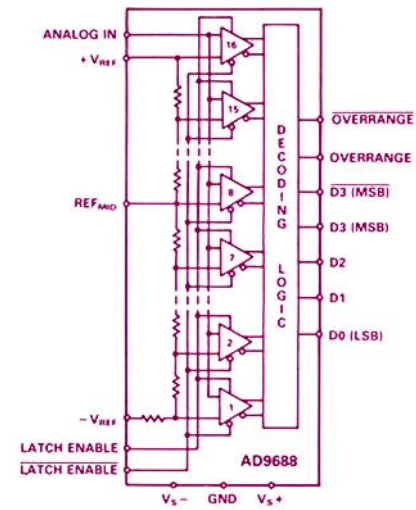


The AD9688* is a 4-bit, high-speed analog-to-digital converter with ECL-compatible outputs. Fabricated in a high-performance bipolar process, it allows full Nyquist operation at up to 200-Msps encoding rates.

With 7-bit linearity (0.0625 LSB for a 4-bit device) and a wide input range (−2.7 V to +3.3 V), it permits devices to be stacked for higher resolutions. Stacking is aided by Overrange output terminals, which can be used to drive decoding logic.

Its 16 high-speed comparators will track input signals at up to 200 MHz. The comparator sampling is controlled by a differential Latch Enable input, designed to be driven by 10K or 100K ECL logic families. The open-emitter outputs employ off-chip pull-down resistors, thus keeping the chip's power dissipation at 700 mW.

Packaged in an 18-pin ceramic DIP, the AD9688 is available for both industrial (AD9688BQ, −25 to +85°C) and military (TQ, −55 to +125°C) temperature ranges. The extended-temperature-range version is also available in a ceramic LCC package. Prices (25+) start at $20.



*Use the reply card for technical data.

Worth Reading

DATABOOKS & SHORT FORMS

DSP Products Databook.* 422 pages of *free* technical data on products for number crunching and digital signal processing. Included are DSP microprocessors, microcoded support components, floating-point components, and fixed-point components. Contains comprehensive data sheets, selection guides, application notes, and other useful information.

Industrial Automation Products Catalog (1987).* Over 200 pages of free technical information on bus-based I/O boards, measurement and control subsystems & systems, and fully integrated systems for factory data acquisition and machine vision.

SERIALS

Analog Briefings—The Newsletter for the Military/Avionics Industry. Volume III, No. 3 discusses radiation hardening in ICs; addition of our Computer Labs Division to the MIL-STD-1772 Qualified Manufacturers list; qualification of our AD2700 voltage-reference families to Military Drawing 85030; 883B processing of our AD586 monolithic voltage reference; and corrections to the *Military Products Databook*. For a free copy, and to subscribe, get in touch with the nearest ADI sales office.

DSPatch—The Digital Signal Processing Newsletter. Numbers 5 and 6 are now available. #5 (16 pp.) features a family portrait of ADI's floating-point components, customer applications, and much more. #6 (16 pp.) features the development tools supporting the ADSP-2100 single-chip DSP µP, a description in some detail of a customer's evaluation process in picking the ADSP-2100, DSP bulletin-board service, and much more. For a free copy, and to subscribe, get in touch with the nearest ADI sales office.

APPLICATION NOTES

Using the AD9610 Transimpedance Amplifier,* by the Technical Staff of ADI's Computer Labs Division (8 pages).

ADG201/202A and ADG221/222 (Switch) Performance with Reduced Power Supplies,* by John Reidy (4 pages).

CMOS DACs and Op Amps Combine to Build Programmable-Gain Amplifiers,* by John Wynne (Parts I and II: 12 + 12 pages).

Interfacing the AD7572 to High-Speed DSP Processors,* by John Reidy (4 pages).

A Guide to Designing Microcoded Circuits,* by Bob Fine (8 pages).

Implement a Writeable Control Store in Your Word-Slice™ System,* by Bob Fine (6 pages).

Variable Width Bit-Reversing with the ADSP-1410 Address Generator,* by Bob Fine (4 pages).

ADI AUTHORS IN THE TRADE PRESS

"Testing ADCs with DSP," by Pat Meehan, *EDN*, October 12, 1987. Dynamic testing of ADCs. [Reprints not available]

"Monolithic R/D Converters," by John Sylvan, *Machine Design*, October 22, 1987. [Reprints not available]

"Transimpedance Amplifiers Minimize Design Tradeoff," by Alan Hansford, *EDN*, November 26, 1987. Transimpedance amplifiers, unlike standard voltage-input designs, maintain constant bandwidth regardless of the gain setting. You can use these amplifiers in video-speed and RF circuitry without having to decrease the gain at high frequencies, while maintaining good dc performance and low power consumption. [Reprints not available]

*Use the reply card for a free copy.

MORE AUTHORS *(Continued from page 2)*

Geoffrey Haigh (page 9) is a Senior Staff Engineer with the Industrial Products Division of ADI, where he is currently working on high-precision and high-speed ADCs and DACs. Before joining ADI, Geoff was a Senior Engineer and Technical Director with Analogic Corp., developing conversion products and medical instruments. Earlier, he designed measurements and analytical instruments at QuanTech Laboratories and Princeton Applied Research Corporation. He has a BS degree from Drew University and more than 20 patents to his credit.

Trevor Emmens (page 6) is a Senior Marketing Engineer with Analog Devices, B.V., in Limerick, Ireland. He has a B.Sc. in Electronic Engineering from the University of Leeds (U.K.) Before joining Analog Devices in 1982, he worked in the audio industry, as Editor of *Elektor Electronics* magazine and as a Product Marketing Engineer with Ferranti Electronics. He enjoys classical music, model-making, gardening, and tennis.

Mike Byrne (page 3) is a Senior Applications Engineer at Analog Devices, B. V., in Limerick, Ireland. He was graduated from the National Institute for Higher Education (Limerick) with a Bachelor of Science degree in Electronic Systems. His spare-time activities include outdoor sports and music.

JoAnn P. Close (page 22) is a Project Engineer in the Linear Design group at Analog Devices Semiconductor. She joined ADS in 1982 after earning a BSEE from MIT and has been responsible for the design and development of precision FET-input amplifier products. Her current interests include low-noise and low-input-current circuits and biomedical electronics. She is an active amateur flute player and a volleyball fanatic.

Alan Hansford (page 16) is a Marketing Engineer at ADI's Computer Labs Division in Greensboro, North Carolina. A biographical sketch and his photo appear in the last issue.

Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

PRODUCT NOTES . . . MCComm-VMS & NOS-VMS are now available to facilitate communications between ADI's **µMAC-5000 & µMAC-6000** and DEC VAX and MicroVAX families . . . The **AD667** 12-Bit DAC has been greatly improved. Significant changes: Input bit currents decrease to 10 µA; power-supply sensitivity decreases to 10 ppm FSR/%; but positive supply current increases to 12 mA. For a copy of the *Product/Process Change Notice*, get in touch with our nearest sales office . . . **DAS1157/8/9:** minimum A/D trigger pulsewidth on data sheet (C849-9-5/84) is incorrect. Max spec of 1 µs in 1986 *Update And Selection Guide* (p. 4-17) is correct, but incomplete. Required pulsewidth is inverse function of voltage, dropping from 900 ns @ 2 V to 500 ns @ 3.6 V (750 µA min) to 300 ns at 5 V; use CMOS, HC, or HCT logic . . . The **AD9610** High-Speed Op Amp is tolerant of (will survive) overdrive up to and beyond V_{IN} x gain = 36V . . . **5B Series: Sockets for single modules (5B03) and pairs (5B04) now available.** Include screw terminals for field wiring, CJC sensors for thermocouples, etc. . . . **MACSYM 200, 250, 260:** CLK03 battery-backed calendar/clock cards have a new battery; they are renamed CLK03A . . . Our **DSP Applications Group has established a computerized Bulletin Board System (BBS).** It has data sheets and app notes; customers can upload and download programs and product information. The phone number is **(617) 528-5012** and parameters are: 8 data bits, no parity, 1 stop bit . . . **AD7572 and AD7672 protection:** Noisy power supplies that transiently exceed absolute max ratings can cause permanent damage. If you're not sure about your power supply, connect a voltage transient absorber (TransZorb—from General Semiconductor Industries, Inc.) MPTE-22 (1N6379) between VDD and VSS, observing proper polarity . . . The **SNAPSHOT** software family, developed by HEM Data Corporation, is for real-time data-acquisition/analuysis; when used with **RTI-800/815 I/O cards,** they turn an IBM PC into a digital oscilloscope. They are available from Analog Devices as **AC1911** (SNAPSHOT STORAGE SCOPE) and **AC1912** (SNAP-FFT), data on request.

IN THE LAST ISSUE

Volume 21, Number 1, 1987 – 32 Pages

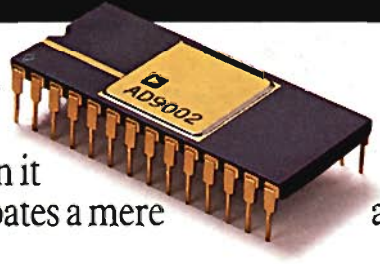
NEW AND REVISED DATA SHEETS AVAILABLE . . . Preliminary data, **ADSP-7018/8018** 16 x 16 Bipolar Multiplier . . . **AC1527-A/AC1527-B** MS-DOS Driver packages for **RTI-800** Series of IBM-compatible I/O products. Also available (new) September, 1987 "**RTI-800** Series Software Guide" . . . **AD558** Low-Cost µP-Compatible 8-Bit DAC; includes **PLCC and Dice info,** updated timing specs & timing diagrams . . **HTC-0300A** Track-and-Hold . . **HDS-1250DAC** . . . **AD7245:** A change in the AD7245's recommended reference-decoupling circuit will be found in the new combined data sheet for **AD7245/AD7248** . . . A change in reference-decoupling recommendations for the **AD7572** will be found in the new data sheet . . **AD7824/7828** data sheet: Address inputs are latched on *rising* edge of RD, contrary to text and Figs. 14 & 15. Also RDY status output is gated internally with CS (not RD). New data sheet reflects implications of these changes.

ERRATA . . . In *1987 Short-Form Selection Guide*, page 139, the following products should have been listed as "Still Available": **AD7110, AD7520, AD7521, AD7530, AD7531, AD7541, AD7546, AD7550, AD7574, AD7581.** The following products, which were listed on page 139, should have been listed on page 140 as "No Longer Available": **AD7115, AD7513, AD7519, AD7527, AD7544, AD7570, AD7583.** Page 78: The **AD7576** has no track/hold; its conversion time is 10 µs, not 5 µs. Page 84: **AD7672** grades & specs tabulated at bottom of page are incorrect; refer to data sheet for correct values . . . **AD9003** data sheet: Fig. 5, p. 7, PNP 2N3906 lower right should be NPN3904 . . . **AD9610** Application Note, equation A. on front page should read: $-V_o = A(\omega)V_s$ . . . **AD1175K** data sheet, specifications: an errata sheet is available; call sales office.

STANDARDS/MILITARY . . . ADI floating-point components (ADSP-32xx) conform to Berkeley test vectors (designed for verifying compliance with **ANSI/IEEE Std 754-1985**) . . . **Standard Military Drawing (SMD) for AD7572** ADC family: **5962-87591,** available from the Naval Publications & Forms Center, 5801 Tabor Ave., Philadelphia PA 19120 . . . **AD578/883B family available.** No missing codes from -55°C to +125°C . . . **AD2700 Series** Precision Voltage References now on **DESC drawing 85030 (rev. A)** . . . **MIL-STD 883** versions of **AD9000 6-Bit Flash ADC** now available . . . **AD7226** quad 8-bit DAC (specifically, **AD7226TQ/883B) now available to SMD: 5962-8780201RX** . . . **AD586 & AD587** 5-V & 10-V references available with **MIL-STD-883B** screening.

PATENTS . . . 4,678,936 to Peter R. Holloway for MOS-Cascoded Bipolar Current Sources in Non-Epitaxial Structure . . **4,685,200 to Delip R. Bokil** for Focused-Heat Sealing of Packages . . . **4,707,682 to Adrian P. Brokaw and Modesto A. Maidique** for A-to-D Converter of the Successive-Approximation Type . . . **4,709,167 to Adrian P. Brokaw** for Three-State Buffer with Anti-Saturation Control.

OUR LIGHTNING-QUICK FLASH CONVERTER IS SO HOT BECAUSE IT'S SO COOL.



When an 8-bit flash converter operates at a blazing sampling rate of 150 MHz, that's hot. When it does it in a 28-pin DIP that dissipates a mere 750mW, that's cool.

Add to that the AD9002's bandwidth of 115MHz and an ultra-low input capacitance of 17pF that simplify your amplifier and system design.

All you need is a single −5.2V power supply, which eliminates latch-up problems. Both military and industrial versions are available.

For more information on our new AD9002 flash converter, contact your nearest Analog Devices sales office.

And be cool.

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The Designer's Advantage.

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